Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4108 1.80 GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECsaind2017_fp_base</th>
<th>SPECsaind2017_fp_peak</th>
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</thead>
<tbody>
<tr>
<td>603.bwaves_s 16</td>
<td>65.9</td>
<td>Not Run</td>
</tr>
<tr>
<td>607.cactuBSSN_s 16</td>
<td>50.6</td>
<td></td>
</tr>
<tr>
<td>619.lbm_s 16</td>
<td>55.7</td>
<td></td>
</tr>
<tr>
<td>627.cam4_s 16</td>
<td>31.6</td>
<td></td>
</tr>
<tr>
<td>628.pop2_s 16</td>
<td>44.0</td>
<td></td>
</tr>
<tr>
<td>638.imagick_s 16</td>
<td>38.4</td>
<td></td>
</tr>
<tr>
<td>644.nab_s 16</td>
<td>67.9</td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s 16</td>
<td>61.7</td>
<td></td>
</tr>
<tr>
<td>654.roms_s 16</td>
<td>65.3</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4108
- **Max MHz:** 3000
- **Nominal:** 1800
- **Enabled:** 16 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 11 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 600G SAS 10K RPM
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
  4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.1 released Oct-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
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SPECspeed®2017_fp_base = 62.2
SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
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<td>16</td>
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<td>314</td>
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<tr>
<td>619.lbm_s</td>
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<tr>
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<td>31.6</td>
<td>281</td>
<td>31.6</td>
</tr>
<tr>
<td>628.pop2_s</td>
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<td>268</td>
<td>44.2</td>
<td>270</td>
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<tr>
<td>638.imagick_s</td>
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<td>38.4</td>
<td>377</td>
<td>38.3</td>
<td>375</td>
<td>38.5</td>
</tr>
<tr>
<td>644.nab_s</td>
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<td>257</td>
<td>67.9</td>
<td>257</td>
<td>67.9</td>
<td>258</td>
<td>67.8</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
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<td>148</td>
<td>61.7</td>
<td>148</td>
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<tr>
<td>654.roms_s</td>
<td>16</td>
<td>242</td>
<td>65.0</td>
<td>240</td>
<td>65.6</td>
<td>241</td>
<td>65.3</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Performance Tuning set to OS Controls</td>
</tr>
<tr>
<td>SNC set to Disabled</td>
</tr>
<tr>
<td>Patrol Scrub set to Disabled</td>
</tr>
<tr>
<td>Sysinfo program /home/cpu2017/bin/sysinfo</td>
</tr>
<tr>
<td>Rev: r5797 of 2017-06-14 96c45e4566354c135fd618bccc09c0f</td>
</tr>
<tr>
<td>running on linux-dkz7 Thu Dec 20 07:39:58 2018</td>
</tr>
</tbody>
</table>

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo:

- **model name**: Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
- **2 "physical id"s (chips)**
- **16 "processors"**

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- **cpu cores**: 8
- **siblings**: 8
- **physical 0: cores 0 1 2 3 4 5 6 7**
- **physical 1: cores 0 1 2 3 4 5 6 7**

From lscpu:

- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **CPU(s)**: 16
- **On-line CPU(s) list**: 0-15
- **Thread(s) per core**: 1
- **Core(s) per socket**: 8
- **Socket(s)**: 2
- **NUMA node(s)**: 2
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 85
- **Model name**: Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
- **Stepping**: 4
- **CPU MHz**: 1646.535
- **CPU max MHz**: 3000.0000
- **CPU min MHz**: 800.0000
- **BogoMIPS**: 3591.54
- **Virtualization**: VT-x
- **L1d cache**: 32K
- **L1i cache**: 32K
- **L2 cache**: 1024K
- **L3 cache**: 11264K
- **NUMA node0 CPU(s)**: 0-7
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4108 1.80 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 62.2
SPECspeed®2017_fp_peak = Not Run

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmrperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtopr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epbi invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_ktg_req intel_pt rsb_cxtsx spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erts invpcid rtl cqm mpx avx512f avx512dq rdseed adx smap clflushopt
c1wb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 385626 MB
node 0 free: 381355 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 387054 MB
node 1 free: 383322 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 791225628 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4108 1.80 GHz)

**SPEC CPU®2017 Floating Point Speed Result**

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Cisco Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Oct-2018</td>
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</tbody>
</table>

**Platform Notes (Continued)**

```
uname -a:
    Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 20 01:17

SPEC is set to: /home/cpu2017
    Filesystem   Type  Size  Used Avail Use% Mounted on
    /dev/sda2     xfs   500G  124G  377G  25% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
    Memory:
        12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400
        12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400
```

**Compiler Version Notes**

```
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
(Continued on next page)
## Cisco Systems

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<td>Oct-2018</td>
</tr>
</tbody>
</table>

### Compiler Version Notes (Continued)

```plaintext
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
----------------|
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

### Base Compiler Invocation

**C benchmarks:**
```
icc -m64 -std=c11
```

**Fortran benchmarks:**
```
ifort -m64
```

**Benchmarks using both Fortran and C:**
```
ifort -m64 icc -m64 -std=c11
```

**Benchmarks using Fortran, C, and C++:**
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
SPEC CPU®2017 Floating Point Speed Result

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CPU2017 License: 9019
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Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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