# SPEC CPU® 2017 Floating Point Speed Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>78.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

### Threads

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base (78.7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s 20</td>
</tr>
<tr>
<td>607.cactuBSSN_s 20</td>
</tr>
<tr>
<td>619.lbm_s 20</td>
</tr>
<tr>
<td>621.wrf_s 20</td>
</tr>
<tr>
<td>627.cam4_s 20</td>
</tr>
<tr>
<td>628.pop2_s 20</td>
</tr>
<tr>
<td>638.imagick_s 20</td>
</tr>
<tr>
<td>644.nab_s 20</td>
</tr>
<tr>
<td>649.fotonik3d_s 20</td>
</tr>
<tr>
<td>654.roms_s 20</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4114
- **Max MHz:** 3000
- **Nominal:** 2200
- **Enabled:** 20 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 600G SAS 10K RPM
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.1 released Oct-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Base</td>
<td></td>
<td></td>
<td>Peak</td>
<td></td>
</tr>
<tr>
<td>603.bwaves_s</td>
<td>20</td>
<td>169</td>
<td>350</td>
<td>169</td>
<td>349</td>
<td>169</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>20</td>
<td>196</td>
<td>85.1</td>
<td>197</td>
<td>84.8</td>
<td>196</td>
<td>85.0</td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>20</td>
<td>77.5</td>
<td>67.6</td>
<td>77.2</td>
<td>67.8</td>
<td>77.3</td>
<td>67.8</td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>20</td>
<td>183</td>
<td>72.3</td>
<td>184</td>
<td>71.9</td>
<td>183</td>
<td>72.1</td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>20</td>
<td>197</td>
<td>44.9</td>
<td>197</td>
<td>45.0</td>
<td>198</td>
<td>44.8</td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>20</td>
<td>216</td>
<td>55.0</td>
<td>216</td>
<td>55.0</td>
<td>216</td>
<td>55.0</td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>20</td>
<td>259</td>
<td>55.7</td>
<td>258</td>
<td>55.8</td>
<td>259</td>
<td>55.7</td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>20</td>
<td>175</td>
<td>99.7</td>
<td>175</td>
<td>99.7</td>
<td>175</td>
<td>99.6</td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>20</td>
<td>138</td>
<td>65.9</td>
<td>154</td>
<td>59.4</td>
<td>147</td>
<td>62.2</td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>20</td>
<td>215</td>
<td>73.1</td>
<td>215</td>
<td>73.2</td>
<td>215</td>
<td>73.3</td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 78.7
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

**SPEC speed®2017_fp_base = 78.7**

**SPEC speed®2017_fp_peak = Not Run**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-dkz7 Wed Dec 12 17:22:05 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
  2 "physical id"s (chips)
  20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 10
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```plaintext
Architecture:         x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              20
On-line CPU(s) list: 0-19
Thread(s) per core:  1
Core(s) per socket:  10
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz
Stepping:            4
CPU MHz:             1881.996
CPU max MHz:         3000.000
CPU min MHz:         800.000
BogoMIPS:            4389.66
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            14080K
NUMA node0 CPU(s): 0-9
```

(Continued on next page)
### SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**  
Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>78.7</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Dec-2018</td>
<td>Aug-2017</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

- NUMA node1 CPU(s): 10-19
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtdesc
- lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
- aperfmperf eagerfpu npi pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
- fma cx16 xtrr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
- xsave avx f16c rdrand lahf_lm abml 3dnowprefetch ida arat epb invpcid_single pln pts
- dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxtsw spec_ctrl stibp
- repoteline kaiser tpr_shadow vnumi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
- avx2 smep bmi2 erms invpcid rtm cmq mpx avx512f avx512dq rdseed adx smap clflushopt
- clwb avx512cd avx512bw avx512vl xsaveopt xsaveopt xsavec xgetbv1 cmq_llc cmq_occulllc

/proc/cpuinfo cache data
- cache size: 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9
- node 0 size: 385626 MB
- node 0 free: 381254 MB
- node 1 cpus: 10 11 12 13 14 15 16 17 18 19
- node 1 size: 387054 MB
- node 1 free: 383483 MB
- node distances:
  - node 0 1
  - 0: 10 21
  - 1: 21 10

From /proc/meminfo
- MemTotal: 791225612 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- SuSE-release:
  - SUSE Linux Enterprise Server 12 (x86_64)
  - VERSION = 12
  - PATCHLEVEL = 2
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check /etc/os-release for details about this release.
- os-release:
  - NAME="SLES"
  - VERSION="12-SP2"
  - VERSION_ID="12.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  - ID="sles"

(Continued on next page)
### SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 78.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Oct-2018

**Platform Notes (Continued)**

```
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:  
Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)  
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 12 11:06
```

```
SPEC is set to: /home/cpu2017
```

```
Filesysten Type  Size  Used  Avail  Use%  Mounted on
/dev/sda2      xfs   500G  124G  377G  25%  /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018**

**Memory:**

- 12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400
- 12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

### Compiler Version Notes

```
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

```
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

```
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

SPECspeed®2017_fp_base = 78.7
SPECspeed®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C
621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
# SPEC CPU®2017 Floating Point Speed Result

## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114 2.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>78.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

### Base Optimization Flags

**C benchmarks:**
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-qopenmp`  
- `-DSPEC_OPENMP`

**Fortran benchmarks:**
- `-DSPEC_OPENMP`  
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-qopenmp`  
- `-nstandard-realloc-lhs`  
- `-align array32byte`

**Benchmarks using both Fortran and C:**
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nstandard-realloc-lhs`  
- `-align array32byte`

**Benchmarks using Fortran, C, and C++:**
- `xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=3`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-nstandard-realloc-lhs`  
- `-align array32byte`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


---

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-12 20:22:05-0500.  
Report generated on 2020-09-04 14:37:01 by CPU2017 PDF formatter v6255.  
Originally published on 2019-01-29.