### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed2017_int_base</th>
<th>SPECspeed2017_int_peak</th>
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<tr>
<td>600.perlbench_s</td>
<td>16</td>
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<td>602.gcc_s</td>
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<td>605.mcf_s</td>
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<td>625.x264_s</td>
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<tr>
<td>657.xz_s</td>
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</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018  

**Hardware**

- **CPU Name:** Intel Xeon Gold 6144  
- **Max MHz.:** 4200  
- **Nominal:** 3500  
- **Enabled:** 16 cores, 2 chips  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 24.75 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)  
- **Storage:** 1 x 600 GB SAS HDD, 15K RPM  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++  
- **Compiler for Linux:**  
- **Fortran:** Version 19.0.1.144 of Intel Fortran  
- **Compiler for Linux:**  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.1 released Oct-2018  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

SPEC CPU2017 Integer Speed Result
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SPECspeed2017_int_base = 9.79
SPECspeed2017_int_peak = 10.1

Results Table

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</tbody>
</table>

**SPECspeed2017_int_base** = 9.79
**SPECspeed2017_int_peak** = 10.1

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32: /home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Platform Notes**

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-dkz7 Wed Dec 5 22:21:44 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
  "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
  siblings : 8
  physical 0: cores 0 2 3 9 16 19 26 27
  physical 1: cores 0 2 3 9 16 19 26 27
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz
Stepping: 4
CPU MHz: 2853.229
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6983.59
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
```

(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6144  
3.50 GHz)  

**SPEC CPU2017 Integer Speed Result**

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---

**Cisco Systems**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018

---

### Platform Notes (Continued)

- **L2 cache:** 1024K  
- **L3 cache:** 25344K  
- **NUMA node0 CPU(s):** 0-7  
- **NUMA node1 CPU(s):** 8-15  
- **Flags:** fpu vme de pse tm mce cx8 apic sep mtrr pge mca cmov  
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp  
  lm constant_tsc art arch_perfmon pebs bts rep_good ntopology nonstop_tsc  
  aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg  
  fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes  
  xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat ptes dtherm hwcap hwlp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp  
  retpoline kaiser tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle  
  avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt  
  clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc  
  /proc/cpuinfo cache data  
  cache size : 25344 KB  

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
- available: 2 nodes (0-1)  
- node 0 cpus: 0 1 2 3 4 5 6 7  
- node 0 size: 385626 MB  
- node 0 free: 385156 MB  
- node 1 cpus: 8 9 10 11 12 13 14 15  
- node 1 size: 387054 MB  
- node 1 free: 386624 MB  
- node distances:  
  node 0 1  
  0: 10 21  
  1: 21 10  

From /proc/meminfo  
MemTotal: 791225628 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*  
**SuSE-release:**  
- SUSE Linux Enterprise Server 12 (x86_64)  
- VERSION = 12  
- PATCHLEVEL = 2  
  # This file is deprecated and will be removed in a future service pack or release.  
  # Please check /etc/os-release for details about this release.  
- **os-release:**  
  - NAME="SLES"  
  - VERSION="12-SP2"  

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

SPECspeed2017_int_base = 9.79
SPECspeed2017_int_peak = 10.1

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 5 22:20

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2      xfs   500G  118G  383G  24% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
    Memory:
        12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
        12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes
---------------------------------------------------------------------------------------
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base, peak) 657.xz_s(base)
---------------------------------------------------------------------------------------
ICC (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---------------------------------------------------------------------------------------

---------------------------------------------------------------------------------------
CC  600.perlbench_s(peak) 602.gcc_s(peak) 605.mcf_s(peak) 625.x264_s(base, peak) 657.xz_s(peak)
---------------------------------------------------------------------------------------
ICC (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
---------------------------------------------------------------------------------------

CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

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**Tested by:** Cisco Systems

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<td>Oct-2018</td>
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---

**Compiler Version Notes (Continued)**

```plaintext
641.leela_s(base)
```

---

```plaintext
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

```plaintext
CXXC 620.omnetpp_s(peak) 623.xalancbmk_s(peak) 631.deepsjeng_s(peak)
641.leela_s(peak)
```

---

```plaintext
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

```plaintext
FC 648.exchange2_s(base, peak)
```

---

```plaintext
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

**Base Compiler Invocation**

C benchmarks:
```plaintext
icc -m64 -std=c11
```

C++ benchmarks:
```plaintext
icpc -m64
```

Fortran benchmarks:
```plaintext
ifort -m64
```

---

**Base Portability Flags**

```plaintext
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
```

(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

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</table>

### Base Portability Flags (Continued)

- **657.xz_s**: `-DSPEC_LP64`

### Base Optimization Flags

- **C benchmarks**: 
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP`
  - `-L/home/cpu2017/je5.0.1-64/ -ljemalloc`

- **C++ benchmarks**: 
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

- **Fortran benchmarks**: 
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
  - `-L/home/cpu2017/je5.0.1-64/ -ljemalloc`

### Peak Compiler Invocation

- **C benchmarks**: 
  - `icc -m64 -std=c11`

- **C++ benchmarks (except as noted below)**: 
  - `icpc -m64`
  - `623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32`

- **Fortran benchmarks**: 
  - `ifort -m64`

### Peak Portability Flags

- **600.perlbench_s**: `-DSPEC_LP64 -DSPEC_LINUX_X64`
- **602.gcc_s**: `-DSPEC_LP64`
- **605.mcf_s**: `-DSPEC_LP64`
- **620.omnetpp_s**: `-DSPEC_LP64`
- **623.xalancbmk_s**: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
- **625.x264_s**: `-DSPEC_LP64`

(Continued on next page)
SPEC CPU2017 Integer Speed Result

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Peak Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6144 3.50 GHz)

SPECspeed2017_int_base = 9.79
SPECspeed2017_int_peak = 10.1

Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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