Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

Test Sponsor: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Score</th>
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</thead>
<tbody>
<tr>
<td>bwaves_s</td>
<td>603</td>
</tr>
<tr>
<td>cactuBSSN_s</td>
<td>607</td>
</tr>
<tr>
<td>lbm_s</td>
<td>619</td>
</tr>
<tr>
<td>wrf_s</td>
<td>621</td>
</tr>
<tr>
<td>cam4_s</td>
<td>627</td>
</tr>
<tr>
<td>pop2_s</td>
<td>628</td>
</tr>
<tr>
<td>imagick_s</td>
<td>638</td>
</tr>
<tr>
<td>nab_s</td>
<td>644</td>
</tr>
<tr>
<td>fotonik3d_s</td>
<td>649</td>
</tr>
<tr>
<td>roms_s</td>
<td>654</td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base (133)

Hardware
CPU Name: Intel Xeon Gold 6154
Max MHz.: 3700
Nominal: 3000
Enabled: 36 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
Cache L2: 1 MB I+D on chip per core
Cache L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 600 GB SAS HDD.15K RPM
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
4.4.120-92.70-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.1.144 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.1 released Oct-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
</tr>
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<tbody>
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<td>122</td>
<td>482</td>
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<td>649.fotonik3d_s</td>
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<td>79.9</td>
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<td>115</td>
<td>137</td>
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<td>138</td>
<td>114</td>
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<td></td>
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</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6154
3.00 GHz)

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bdc091c0f
running on linux-dkz7 Wed Dec 5 04:12:52 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6154 CPU @ 3.00GHz
  2  "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6154 CPU @ 3.00GHz
Stepping: 4
CPU MHz: 2958.499
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5985.90
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17

(Continued on next page)
**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

| SPECs| 2017 fp_base = | 133 |
| SPECs| 2017 fp_peak = | Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Platform Notes (Continued)**

NUMA node1 CPU(s): 18-35

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrr pdcm pcdrc dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
rtpoline kaiser tpr_shadow vmmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cmq mpx avx512f avx512dq rsdsev adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cmq_llc cmq_occup_llc

/procd/cpuinfo cache data
  cache size: 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
  node 0 size: 385626 MB
  node 0 free: 382037 MB
  node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
  node 1 size: 387054 MB
  node 1 free: 382574 MB
  node distances:
    node   0   1
    0:  10  21
    1:  21  10

From /proc/meminfo
  MemTotal: 791225548 KB
  HugePages_Total: 0
  Hugepagesize: 2048 KB

From /etc/*release*/etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 4 23:15

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 500G 124G 377G 25% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018
Memory:
  12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
  12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC 607.cactuBSSN_s(base)
==============================================================================
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

SPECspeed2017_fp_base = 133
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Compiler Version Notes (Continued)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

==============================================================================
CC 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
==============================================================================
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
## SPEC CPU2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6154 3.00 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
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<tr>
<td>SPECspeed2017_fp_peak</td>
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</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Oct-2018

### Base Optimization Flags

**C benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

**Benchmarks using Fortran, C, and C++:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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