Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

<table>
<thead>
<tr>
<th>Name</th>
<th>Threads</th>
<th>SPECspeed2017_fp_base (172)</th>
</tr>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>96</td>
<td>223</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>96</td>
<td>82.6</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>96</td>
<td>76.8</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>96</td>
<td>144</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>96</td>
<td>52.2</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>96</td>
<td>215</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>96</td>
<td>424</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>96</td>
<td>110</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>96</td>
<td>263</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>96</td>
<td>82</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Platinum 8160M
Max MHz.: 3700
Nominal: 2100
Enabled: 96 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 33 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
Compiler for Linux;
Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Nov-2018  
Hardware Availability: Aug-2017  
Software Availability: Mar-2018

Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>71.9</td>
<td>820</td>
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<td>75.0</td>
<td>222</td>
<td>74.6</td>
<td>224</td>
<td>74.9</td>
<td>223</td>
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<tr>
<td>619.lbm_s</td>
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<td>63.2</td>
<td>82.9</td>
<td>63.4</td>
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<td>82.3</td>
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<td>61.5</td>
<td>144</td>
<td>61.6</td>
<td>144</td>
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<td>628.pop2_s</td>
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<td>225</td>
<td>52.7</td>
<td>227</td>
<td>52.2</td>
<td>229</td>
<td>51.8</td>
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<td>67.2</td>
<td>215</td>
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<td>213</td>
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<td>424</td>
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<td>425</td>
<td>41.3</td>
<td>423</td>
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<td>96</td>
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<td>111</td>
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<td>110</td>
<td>84.5</td>
<td>108</td>
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<td>654.roms_s</td>
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<td>61.7</td>
<td>255</td>
<td>59.9</td>
<td>263</td>
<td>59.8</td>
<td>263</td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 172  
SPECspeed2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

| SPECspeed2017_fp_base | 172 |
| SPECspeed2017_fp_peak | Not Run |

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Test Date:** Nov-2018

**Tested by:** Cisco Systems

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

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**Platform Notes**

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

**Sysinfo program /opt/cpu2017/bin/sysinfo**

```
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-vb5q Sun Nov 18 00:48:45 2018
```

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Platinum 8160M CPU @ 2.10GHz
4 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8160M CPU @ 2.10GHz
Stepping: 4
CPU MHz: 3626.567
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4199.99
Virtualization: VT-x
```

(Continued on next page)
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Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPEC CPU2017 Floating Point Speed Result

SPECspeed2017_fp_base = 172
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
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Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 33792K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
NUMA node2 CPU(s): 48-71
NUMA node3 CPU(s): 72-95
Flags: fpu vme de pse mtrr pmxs cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good ntopology nonstop_tsc
aperfmon perf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epbt invpncd_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pms_req intel_pt spec_ctrl kaiser tpr_shadow
vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpdcrd rtc mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavesel xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data
cache size : 33792 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
nod 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 385463 MB
node 0 free: 380425 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387057 MB
node 1 free: 384273 MB
node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 2 size: 387057 MB
node 2 free: 381891 MB
node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 387054 MB
node 3 free: 383448 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 1583751156 kB
HugePages_Total: 0

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

SPEC CPU2017 Floating Point Speed Result
Copyright 2017-2018 Standard Performance Evaluation Corporation

SPECspeed2017_fp_base = 172
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
   SUSE Linux Enterprise Server 12 (x86_64)
   VERSION = 12
   PATCHLEVEL = 2
   # This file is deprecated and will be removed in a future service pack or release.
   # Please check /etc/os-release for details about this release.

os-release:
   NAME="SLES"
   VERSION="12-SP2"
   VERSION_ID="12.2"
   PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
   ID="sles"
   ANSI_COLOR="0;32"
   CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 2 21:46

SPEC is set to: /opt/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 90G 190G 33% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
   48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

<table>
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</tbody>
</table>

Specspeed2017_fp_base = 172
Specspeed2017_fp_peak = Not Run

Compiler Version Notes (Continued)

==============================================================================
FC 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
FC 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
CC 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

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Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.hm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -DSPEC_OPENMP -xcORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both Fortran and C:
-Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-Wl,-z,muldefs -xcORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml
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Cisco UCS B480 M5 (Intel Xeon Platinum 8160M, 2.10 GHz)

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