Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPECspeed2017_fp_base = 132
SPECspeed2017_fp_peak = 133

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

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<td>619.lbm_s 32</td>
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<td>628.pop2_s 32</td>
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<tr>
<td>638.imagick_s 32</td>
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<tr>
<td>644.nab_s 32</td>
<td>712</td>
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<tr>
<td>649.fotonik3d_s 32</td>
<td>194</td>
<td>203</td>
</tr>
<tr>
<td>654.roms_s 32</td>
<td>207</td>
<td>203</td>
</tr>
</tbody>
</table>

**Hardware**

CPU Name: Intel Xeon Gold 6134
Max MHz.: 3700
Nominal: 3200
Enabled: 32 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

**Software**

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.103-92.56-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPECspeed2017_fp_base = 132
SPECspeed2017_fp_peak = 133

Results Table

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</table>

SPECspeed2017_fp_base = 132
SPECspeed2017_fp_peak = 133

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPEC CPU2017 Floating Point Speed Result

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SPECspeed2017_fp_base = 132
SPECspeed2017_fp_peak = 133

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /opt/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-vb5q Wed Oct 31 08:25:05 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6134 CPU @ 3.20GHz
  4 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
  physical 0: cores 0 1 2 3 10 11 24 27
  physical 1: cores 1 2 3 4 8 18 24 27
  physical 2: cores 0 2 3 9 16 19 26 27
  physical 3: cores 0 2 3 9 16 19 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6134 CPU @ 3.20GHz
Stepping: 4
CPU MHz: 2674.576
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 6400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K

(Continued on next page)
## Platform Notes (Continued)

- **L3 cache:** 25344K
- **NUMA node0 CPU(s):** 0-7
- **NUMA node1 CPU(s):** 8-15
- **NUMA node2 CPU(s):** 16-23
- **NUMA node3 CPU(s):** 24-31

**Flags:**
- fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
- lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
- aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
- fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
- xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dthr hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow
- vnmi f1epriority ept vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 rome invpcid
- rtm cmp mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw
- avx512vl xsaveopt xsavec xgetbv1 cmp_llc cmp_occup_llc

/proc/cpuinfo cache data
- cache size: 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
- available: 4 nodes (0-3)
- node 0 cpus: 0 1 2 3 4 5 6 7
- node 0 size: 385463 MB
- node 0 free: 382392 MB
- node 1 cpus: 8 9 10 11 12 13 14 15
- node 1 size: 387057 MB
- node 1 free: 383065 MB
- node 2 cpus: 16 17 18 19 20 21 22 23
- node 2 size: 387057 MB
- node 2 free: 382921 MB
- node 3 cpus: 24 25 26 27 28 29 30 31
- node 3 size: 387054 MB
- node 3 free: 381829 MB

node distances:
- node 0 1 2 3
- 0: 10 21 21 21
- 1: 21 10 21 21
- 2: 21 21 10 21
- 3: 21 21 21 10

From /proc/meminfo
- MemTotal: 1583751412 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

---

**Platform Notes (Continued)**

SuSE-release:
- SUSE Linux Enterprise Server 12 (x86_64)
- VERSION = 12
- PATCHLEVEL = 2
- # This file is deprecated and will be removed in a future service pack or release.
- # Please check /etc/os-release for details about this release.

os-release:
- NAME="SLES"
- VERSION="12-SP2"
- VERSION_ID="12.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
- ID="sles"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
- Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
- x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 2 03:28

SPEC is set to: /opt/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 90G 190G 32% /

---

**Compiler Version Notes**

```plaintext
CC 619.lbm_s(base) 638.imagick_s(base, peak) 644.nab_s(base, peak)
```

---

```
icc (ICC) 18.0.0 20170811
```

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

```
CC 619.lbm_s(peak)
```

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

<table>
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<tr>
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<tr>
<td>SPECspeed2017_fp_peak</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

### Compiler Version Notes (Continued)

```plaintext
icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

FC 607.cactuBSSN_s(base)  
icpc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.  
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

FC 607.cactuBSSN_s(peak)  
icpc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.  
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

FC 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)  
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

FC 603.bwaves_s(peak) 649.fotonik3d_s(peak) 654.roms_s(peak)  
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

CC 621.wrf_s(base) 627.cam4_s(base, peak) 628.pop2_s(base)  
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811
```

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPEC CPU2017 Floating Point Speed Result

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Cisco Systems

SPECspeed2017_fp_base = 132
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Compiler Version Notes (Continued)

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---

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPECspeed2017_fp_base = 132
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---

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

---

**Peak Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

---

**Peak Portability Flags**

Same as Base Portability Flags
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

SPECspeed2017_fp_base = 132
SPECspeed2017_fp_peak = 133

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Mar-2018

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml
## SPEC CPU2017 Floating Point Speed Result

### Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6134 3.20 GHz)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.2 on 2018-10-31 08:25:05-0400.
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