Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECspeed2017_fp_base = 157
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

 Threads 0 40 80 120 160 200 240 280 320 360 400 440 480 520 560 600 640 680 720 760 800 840 880
603.bwaves_s 64 607.cactuBSSN_s 64 619.lbm_s 64 621.wrf_s 64 627.cam4_s 64 628.pop2_s 64 638.imagick_s 64 644.nab_s 64 649.fotonik3d_s 64 654.roms_s 64

603.bwaves_s 64
607.cactuBSSN_s 64
619.lbm_s 64
621.wrf_s 64
627.cam4_s 64
628.pop2_s 64
638.imagick_s 64
644.nab_s 64
649.fotonik3d_s 64
654.roms_s 64

Hardware
CPU Name: Intel Xeon Gold 6142M
Max MHz.: 3700
Nominal: 2600
Enabled: 64 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 400 GB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
4.4.103-92.56-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
Compiler for Linux;
Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 3.2.3c released Mar-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECspeed2017_fp_base = 157
SPECspeed2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>64</td>
<td>68.5</td>
<td>861</td>
<td>68.3</td>
<td>863</td>
<td>68.9</td>
<td>856</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>64</td>
<td>84.8</td>
<td>196</td>
<td>85.0</td>
<td>196</td>
<td>84.8</td>
<td>197</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>64</td>
<td>65.2</td>
<td>80.3</td>
<td>65.1</td>
<td>80.4</td>
<td>65.3</td>
<td>80.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>64</td>
<td>174</td>
<td>75.9</td>
<td>170</td>
<td>77.7</td>
<td>171</td>
<td>77.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>64</td>
<td>72.7</td>
<td>122</td>
<td>71.6</td>
<td>124</td>
<td>71.9</td>
<td>123</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>64</td>
<td>266</td>
<td>44.6</td>
<td>286</td>
<td>41.4</td>
<td>305</td>
<td>38.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>64</td>
<td>80.9</td>
<td>178</td>
<td>83.2</td>
<td>173</td>
<td>83.0</td>
<td>174</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>64</td>
<td>47.6</td>
<td>367</td>
<td>47.7</td>
<td>366</td>
<td>47.6</td>
<td>367</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>64</td>
<td>82.3</td>
<td>111</td>
<td>81.3</td>
<td>112</td>
<td>80.0</td>
<td>114</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>64</td>
<td>65.9</td>
<td>239</td>
<td>66.9</td>
<td>235</td>
<td>66.4</td>
<td>237</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed2017_fp_base = 157
SPECspeed2017_fp_peak = Not Run

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3/> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
<th>157</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /opt/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f
running on linux-vb5q Sat Nov 10 19:25:40 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

<table>
<thead>
<tr>
<th>From /proc/cpuinfo</th>
</tr>
</thead>
<tbody>
<tr>
<td>model name: Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz</td>
</tr>
<tr>
<td>4 &quot;physical id&quot;s (chips)</td>
</tr>
<tr>
<td>64 &quot;processors&quot;</td>
</tr>
<tr>
<td>cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)</td>
</tr>
<tr>
<td>cpu cores : 16</td>
</tr>
<tr>
<td>siblings : 16</td>
</tr>
<tr>
<td>physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15</td>
</tr>
<tr>
<td>physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15</td>
</tr>
<tr>
<td>physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15</td>
</tr>
<tr>
<td>physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15</td>
</tr>
</tbody>
</table>

From lscpu:

<table>
<thead>
<tr>
<th>From lscpu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture: x86_64</td>
</tr>
<tr>
<td>CPU op-mode(s): 32-bit, 64-bit</td>
</tr>
<tr>
<td>Byte Order: Little Endian</td>
</tr>
<tr>
<td>CPU(s): 64</td>
</tr>
<tr>
<td>On-line CPU(s) list: 0-63</td>
</tr>
<tr>
<td>Thread(s) per core: 1</td>
</tr>
<tr>
<td>Core(s) per socket: 16</td>
</tr>
<tr>
<td>Socket(s): 4</td>
</tr>
<tr>
<td>NUMA node(s): 4</td>
</tr>
<tr>
<td>Vendor ID: GenuineIntel</td>
</tr>
<tr>
<td>CPU family: 6</td>
</tr>
<tr>
<td>Model: 85</td>
</tr>
<tr>
<td>Model name: Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz</td>
</tr>
<tr>
<td>Stepping: 4</td>
</tr>
<tr>
<td>CPU MHz: 1256.235</td>
</tr>
<tr>
<td>CPU max MHz: 3700.0000</td>
</tr>
<tr>
<td>CPU min MHz: 1000.0000</td>
</tr>
<tr>
<td>BogoMIPS: 5199.95</td>
</tr>
<tr>
<td>Virtualization: VT-x</td>
</tr>
</tbody>
</table>

(Continued on next page)
### Platform Notes (Continued)

- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 22528K
- **NUMA node0 CPU(s):** 0-15
- **NUMA node1 CPU(s):** 16-31
- **NUMA node2 CPU(s):** 32-47
- **NUMA node3 CPU(s):** 48-63
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good ntopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt spec_ctrl kaiser tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  ertz invpcid rtq cmq mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

From `numactl --hardware`:

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385463 MB
node 0 free: 381472 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387057 MB
node 1 free: 385287 MB
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 2 size: 387057 MB
node 2 free: 385790 MB
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 3 size: 387054 MB
node 3 free: 384577 MB
node distances:
node 0  1  2  3
0:  10  21  21  21
1:  21  10  21  21
2:  21  21  10  21
3:  21  21  21  10
```

From `/proc/meminfo`

```
MemTotal: 1583751284 kB
HugePages_Total: 0
```

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPEC CPU2017 Floating Point Speed Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

SPECspeed2017_fp_base = 157
SPECspeed2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-vb5q 4.4.103-92.56-default #1 SMP Wed Dec 27 16:24:31 UTC 2017 (2fd2155)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 11 13:21

SPEC is set to: /opt/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda1 xfs 280G 84G 196G 30% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
  48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
  CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
  icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017 fp_base =</th>
<th>157</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017 fp_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**Spec CPU2017 Floating Point Speed Result**

---

**Compiler Version Notes (Continued)**

```plaintext
FC  607.cactuBSSN_s(base)

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```plaintext
FC  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

```plaintext
CC  621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
```

---

**Base Compiler Invocation**

**C benchmarks:**
icc -m64 -std=c11

**Fortran benchmarks:**
ifort -m64

**Benchmarks using both Fortran and C:**
ifort -m64 icc -m64 -std=c11

**Benchmarks using Fortran, C, and C++:**
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
<th>157</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

---

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byte_recl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-W1,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both Fortran and C:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -L/usr/local/je5.0.1-64/lib -ljemalloc

---

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
## SPEC CPU2017 Floating Point Speed Result

### Cisco Systems

**Cisco UCS B480 M5 (Intel Xeon Gold 6142M 2.60 GHz)**

<table>
<thead>
<tr>
<th>SPECspeed2017_fp_base</th>
<th>157</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Nov-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2018</td>
</tr>
</tbody>
</table>

---

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Originally published on 2018-11-27.