## SPEC® CPU2017 Floating Point Rate Result

**Supermicro**

SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114T)

<table>
<thead>
<tr>
<th>SPECrate2017_fp_base</th>
<th>SPECrate2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>50.1</td>
<td>51.6</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 001176

**Test Sponsor:** Supermicro

**Tested by:** Supermicro

**Test Date:** Oct-2018

**Hardware Availability:** Jul-2017

**Software Availability:** Mar-2018

### Hardware

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
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<tr>
<td>503.bwaves_r</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
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<tr>
<td>510.parest_r</td>
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<td>519.lbm_r</td>
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<td>521.wrf_r</td>
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<tr>
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<td>81.7</td>
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<tr>
<td>549.fotonik3d_r</td>
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<tr>
<td>554.roms_r</td>
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<td>23.1</td>
</tr>
</tbody>
</table>

**SPECrate2017_fp_base (50.1)**

**SPECrate2017_fp_peak (51.6)**

### Software

**OS:** SUSE Linux Enterprise Server 12 SP3 (x86_64)

**Kernel:** 4.4.114-94.11-default

**Compiler:**
- C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;
- Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux

**Parallel:** No

**Firmware:** Supermicro BIOS version 2.1 released Jun-2018

**File System:** xfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** 64-bit

**Other:** None

---

**CPU Name:** Intel Xeon Silver 4114T

**Max MHz.:** 3000

**Nominal:** 2200

**Enabled:** 10 cores, 1 chip, 2 threads/core

**Orderable:** 1 chip

**Cache L1:** 32 KB I + 32 KB D on chip per core

**L2:** 1 MB I+D on chip per core

**L3:** 13.75 MB I+D on chip per core

**Other:** None

**Memory:** 192 GB (6 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)

**Storage:** 1 x 200 GB SATA III SSD

**Other:** None
## Supermicro

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<td>25.3</td>
</tr>
</tbody>
</table>

**SPECrate2017_fp_base = 50.1**

**SPECrate2017_fp_peak = 51.6**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/jn.5.0.1-32:/home/cpu2017/jn.5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
## General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

**BIOS Settings:**
- LLC prefetch = Enable
- Power Technology = Custom
- Power Performance Tuning = BIOS Controls EPB
- ENERGY_PERF_BIAS_CFG mode = Maximum Performance
- Hardware P-state = Out of Band Mode
- XPT Prefetch = Enable
- Stale AtoS = Enable
- LLC dead line alloc = Disable
- SDDC Plus One = Disable
- ADDDC Sparing = Disable
- Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-52ma Sat Oct 20 05:42:55 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Silver 4114T CPU @ 2.20GHz
- 1 "physical id"s (chips)
- 20 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 10
  - siblings : 20
  - physical 0: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 20
- On-line CPU(s) list: 0-19
- Thread(s) per core: 2
- Core(s) per socket: 10
- Socket(s): 1
- NUMA node(s): 1

(Continued on next page)
Supermicro
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Hardware Availability: Jul-2017
Tested by: Supermicro
Software Availability: Mar-2018

Platform Notes (Continued)

Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4114T CPU @ 2.20GHz
Stepping: 4
CPU MHz: 2199.991
BogoMIPS: 4399.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-19
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsdp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsdp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp_epp intel_pt rsb_ctxsw spec_ctrl retpoline kaiser tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertz invpcid rt
mcm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc pku ospke

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 1 nodes (0)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 192078 MB
  node 0 free: 177763 MB
  node distances:
    node 0
    0: 10

From /proc/meminfo
  MemTotal: 196687880 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 3

(Continued on next page)
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Platform Notes (Continued)

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP3"
  VERSION_ID="12.3"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME=cpe:/o:suse:sles:12:sp3"

uname -a:
  Linux linux-52ma 4.4.114-94.11-default #1 SMP Thu Feb 1 19:28:26 UTC 2018 (4309ff9)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Mitigation: PTI
CVE-2017-5753 (Spectre variant 1): Mitigation: Barriers
CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

run-level 3 Oct 19 18:28

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda4      xfs   145G   48G   97G  33% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS American Megatrends Inc. 2.1 06/15/2018
  Memory:
    2x NO DIMM NO DIMM
    6x Samsung M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base, peak)
==============================================================================
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
(Continued on next page)
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Compiler Version Notes (Continued)

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CXXC 508.namd_r(base) 510.parest_r(base, peak)
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icpcc (ICC) 18.0.2 20180210
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icc (ICC) 18.0.2 20180210
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Compiler Version Notes (Continued)

ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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FC  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)
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icc (ICC) 18.0.2 20180210
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

(Continued on next page)
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**Base Compiler Invocation (Continued)**

- **Benchmarks using both Fortran and C:**
  ```
  ifort -m64 icc -m64 -std=c11
  ```

- **Benchmarks using both C and C++:**
  ```
  icpc -m64 icc -m64 -std=c11
  ```

- **Benchmarks using Fortran, C, and C++:**
  ```
  icpc -m64 icc -m64 -std=c11 ifort -m64
  ```

**Base Portability Flags**

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

- **C benchmarks:**
  ```
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3
  ```

- **C++ benchmarks:**
  ```
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3
  ```

- **Fortran benchmarks:**
  ```
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
  ```

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

(Continued on next page)
# SPEC CPU2017 Floating Point Rate Result

**Supermicro**  
**SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114T)**  

<table>
<thead>
<tr>
<th>CPU2017 License: 001176</th>
<th>Test Date: Oct-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Supermicro</td>
<td>Hardware Availability: Jul-2017</td>
</tr>
<tr>
<td>Tested by: Supermicro</td>
<td>Software Availability: Mar-2018</td>
</tr>
</tbody>
</table>

| SPECrate2017_fp_base = 50.1 |
| SPECrate2017_fp_peak = 51.6 |

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## Peak Optimization Flags (Continued)

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

538.imagick_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

544.nab_r: Same as 538.imagick_r

### C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

510.parest_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

### Fortran benchmarks:

503.bwaves_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

### Benchmarks using both Fortran and C:

- `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

### Benchmarks using both C and C++:

511.povray_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

526.blender_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

### Benchmarks using Fortran, C, and C++:

- `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only`
SPEC CPU2017 Floating Point Rate Result
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Supermicro
SuperStorage 5049P-E1CR45H (X11SPL-F, Intel Xeon Silver 4114T)

SPECrate2017_fp_base = 50.1
SPECrate2017_fp_peak = 51.6

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Oct-2018
Hardware Availability: Jul-2017
Software Availability: Mar-2018

Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-SKL-revD.xml

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Tested with SPEC CPU2017 v1.0.5 on 2018-10-19 17:42:54-0400.