Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

SPECspeed®2017_fp_base = 110
SPECspeed®2017_fp_peak = 111

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
<td>CPU Name: Intel Xeon Gold 6140</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
<td>Max MHz: 3700</td>
</tr>
<tr>
<td>Firmware: Version 3.1.1d released Jun-2017</td>
<td>Nominal: 2300</td>
</tr>
<tr>
<td>File System: xfs</td>
<td>Enabled: 36 cores, 2 chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 64-bit</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: None</td>
<td>L3: 24.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: --</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tested by: Cisco Systems</th>
<th>Test Date: Dec-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software Availability: Sep-2017</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (110)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s 36</td>
<td>151</td>
</tr>
<tr>
<td>607.cactuBSSN_s 36</td>
<td>153</td>
</tr>
<tr>
<td>619.ibm_s 36</td>
<td>44.0</td>
</tr>
<tr>
<td>621.wrf_s 36</td>
<td>82.8</td>
</tr>
<tr>
<td>627.cam4_s 36</td>
<td>77.7</td>
</tr>
<tr>
<td>628.pop2_s 36</td>
<td>66.1</td>
</tr>
<tr>
<td>638.imagick_s 36</td>
<td>107</td>
</tr>
<tr>
<td>644.nab_s 36</td>
<td>193</td>
</tr>
<tr>
<td>649.fotonik3d_s 36</td>
<td>193</td>
</tr>
<tr>
<td>654.roms_s 36</td>
<td>113</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_peak (111)</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
</tr>
<tr>
<td>110</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Copyright 2017-2020 Standard Performance Evaluation Corporation
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 110
SPECspeed®2017_fp_peak = 111

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>36</td>
<td>118</td>
<td>500</td>
<td>119</td>
<td>495</td>
<td>119</td>
<td>498</td>
<td>36</td>
<td>118</td>
<td>499</td>
<td>119</td>
<td>499</td>
<td>119</td>
<td>496</td>
</tr>
<tr>
<td>607.cactubssn_s</td>
<td>36</td>
<td>110</td>
<td>151</td>
<td>111</td>
<td>151</td>
<td>111</td>
<td>151</td>
<td>36</td>
<td>109</td>
<td>153</td>
<td>109</td>
<td>153</td>
<td>110</td>
<td>152</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>36</td>
<td>119</td>
<td>43.9</td>
<td>119</td>
<td>44.1</td>
<td>119</td>
<td>44.0</td>
<td>36</td>
<td>119</td>
<td>43.9</td>
<td>119</td>
<td>43.9</td>
<td>119</td>
<td>44.0</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>36</td>
<td>160</td>
<td><strong>82.8</strong></td>
<td>160</td>
<td>82.6</td>
<td>160</td>
<td>82.9</td>
<td>36</td>
<td>151</td>
<td><strong>87.4</strong></td>
<td>152</td>
<td>87.1</td>
<td>151</td>
<td><strong>87.6</strong></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>36</td>
<td>114</td>
<td>77.8</td>
<td><strong>114</strong></td>
<td><strong>77.7</strong></td>
<td>114</td>
<td>77.4</td>
<td>36</td>
<td>120</td>
<td>74.0</td>
<td><strong>117</strong></td>
<td><strong>75.5</strong></td>
<td>114</td>
<td>78.0</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>36</td>
<td>178</td>
<td>66.5</td>
<td><strong>180</strong></td>
<td>66.1</td>
<td>181</td>
<td>65.7</td>
<td>36</td>
<td>181</td>
<td>65.7</td>
<td>177</td>
<td>67.0</td>
<td><strong>179</strong></td>
<td><strong>66.2</strong></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>36</td>
<td>134</td>
<td><strong>107</strong></td>
<td>134</td>
<td>108</td>
<td>137</td>
<td>105</td>
<td>36</td>
<td>138</td>
<td>105</td>
<td>134</td>
<td>107</td>
<td><strong>135</strong></td>
<td><strong>107</strong></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>36</td>
<td>90.5</td>
<td>193</td>
<td>90.4</td>
<td>193</td>
<td><strong>90.5</strong></td>
<td><strong>193</strong></td>
<td>36</td>
<td>90.5</td>
<td>193</td>
<td><strong>90.5</strong></td>
<td><strong>193</strong></td>
<td>90.5</td>
<td>193</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>36</td>
<td>112</td>
<td>81.4</td>
<td>111</td>
<td>82.3</td>
<td><strong>111</strong></td>
<td><strong>81.9</strong></td>
<td>36</td>
<td>112</td>
<td>81.4</td>
<td>113</td>
<td>80.5</td>
<td><strong>113</strong></td>
<td><strong>80.9</strong></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>36</td>
<td>137</td>
<td>115</td>
<td><strong>139</strong></td>
<td>113</td>
<td>139</td>
<td>113</td>
<td>36</td>
<td>133</td>
<td>118</td>
<td><strong>134</strong></td>
<td><strong>118</strong></td>
<td>135</td>
<td>117</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "702M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>/proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly

(Continued on next page)
# SPEC CPU®2017 Floating Point Speed Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>111</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### General Notes (Continued)

generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Disabled
  - Patrol Scrub set to Disabled
  - Sysinfo program /home/cpu2017/bin/sysinfo
  - Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
    running on linux-nvug Thu Dec 21 20:30:29 2017

- **SUT (System Under Test) info as seen by some common utilities.**
  - For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

  From /proc/cpuinfo
  ```
  model name : Intel(R) Xeon(R) Gold 6140 CPU @ 2.30GHz
  2  "physical id"s (chips)
  36 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 18
  siblings : 18
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  ```

  From lscpu:
  ```
  Architecture:          x86_64
  CPU op-mode(s):        32-bit, 64-bit
  Byte Order:            Little Endian
  CPU(s):                36
  On-line CPU(s) list:   0-35
  Thread(s) per core:    1
  Core(s) per socket:    18
  Socket(s):             2
  ```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

SPECspeed®2017_fp_base = 110
SPECspeed®2017_fp_peak = 111

Platform Notes (Continued)

NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6140 CPU @ 2.30GHz
Stepping:              4
CPU MHz:               3373.725
CPU max MHz:           3700.0000
CPU min MHz:           1000.0000
BogoMIPS:              4589.22
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              25344K
NUMA node0 CPU(s):     0-17
NUMA nodel CPU(s):     18-35

Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmlinux flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3msc invpcid rtm cmp cmx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cmp_ia32 cmp_ia32e

From /proc/cpuinfo cache data
cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 192090 MB
node 0 free: 191353 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 193518 MB
node 1 free: 192868 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 394863376 kB

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

 SPECspeed®2017_fp_base = 110
 SPECspeed®2017_fp_peak = 111

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-nvug 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 21 15:10

SPEC is set to: /home/cpu2017
  Filesystem   Type  Size  Used  Avail Use%  Mounted on
  /dev/sda2    xfs   644G  177G  468G  28%  /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
  Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C     | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak) |
==============================================================================

icc (ICC) 18.0.0 20170811

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

<table>
<thead>
<tr>
<th>SPEC®2017_fp_base</th>
<th>SPEC®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>111</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

Compiler Version Notes (Continued)

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

C++, C, Fortran | 607.cactuBSSN_s(base, peak)

---

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak) 654.roms_s(base, peak)

---

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak) 628.pop2_s(base, peak)

---

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

---

Base Compiler Invocation

C benchmarks:
- icc

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icc

Benchmarks using Fortran, C, and C++:
- icpc icc ifort
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

SPECspeed\textsuperscript{\textregistered}2017\textsubscript{fp}\textsubscript{peak} = 111
SPECspeed\textsuperscript{\textregistered}2017\textsubscript{fp}\textsubscript{base} = 110

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Portability Flags

603.bwaves\textsubscript{s}: -DSPEC\_LP64
607.cactuBSSN\textsubscript{s}: -DSPEC\_LP64
619.lbm\textsubscript{s}: -DSPEC\_LP64
621.wrf\textsubscript{s}: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian
627.cam4\textsubscript{s}: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG
628.pop2\textsubscript{s}: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian
-assume byterecl
638.imagick\textsubscript{s}: -DSPEC\_LP64
644.nab\textsubscript{s}: -DSPEC\_LP64
649.fotonik3d\textsubscript{s}: -DSPEC\_LP64
654.roms\textsubscript{s}: -DSPEC\_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC\_OPENMP

Fortran benchmarks:
-DSPEC\_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC\_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

SPECspeed®2017_fp_base = 110
SPECspeed®2017_fp_peak = 111

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Other Flags (Continued)

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

(Continued on next page)
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>110</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>111</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Test Date:** Dec-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Sep-2017

---

### Peak Optimization Flags (Continued)

**Fortran benchmarks:**
- `-prof-gen(pass 1)`  
- `-prof-use(pass 2)`  
- `-DSPEC_SUPPRESS_OPENMP`  
- `-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`  
- `-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -gopenmp`  
- `-nostandard-realloc-lhs -align array32byte`

**Benchmarks using both Fortran and C:**

- 621.wrf_s:
  - `-prof-gen(pass 1)`  
  - `-prof-use(pass 2)`  
  - `-O2 -xCORE-AVX512`  
  - `-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div`  
  - `-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp`  
  - `-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte`

- 627.cam4_s:
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`  
  - `-ffinite-math-only -qopt-mem-layout-trans=3 -gopenmp`  
  - `-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte`

- 628.pop2_s: Same as 621.wrf_s

**Benchmarks using Fortran, C, and C++:**

- `-m64 -std=c11`

---

### Peak Other Flags

**C benchmarks:**
- `-m64 -std=c11`

**Fortran benchmarks:**
- `-m64`

**Benchmarks using both Fortran and C:**
- `-m64 -std=c11`

**Benchmarks using Fortran, C, and C++:**
- `-m64 -std=c11`

---

The flags files that were used to format this result can be browsed at

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6140, 2.30 GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 110</th>
<th>SPECspeed®2017_fp_peak = 111</th>
</tr>
</thead>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml  
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml