## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

**SPECspeed®2017_fp_base = 122**

**SPECspeed®2017_fp_peak = 123**

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<thead>
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<th>CPU2017 License: 9019</th>
<th>Test Date: Dec-2017</th>
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<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2017</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Platinum 8170
  - Max MHz: 3700
  - Nominal: 2100
  - Enabled: 52 cores, 2 chips
  - Orderable: 1,2 Chips
  - Cache L1: 32 KB I + 32 KB D on chip per core
  - Cache L2: 1 MB I+D on chip per core
  - Cache L3: 35.75 MB I+D on chip per chip
  - Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
  - Storage: 1 x 1 TB SAS HDD, 7.2K RPM
  - Other: None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.1d released Jun-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --

### Threads

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<th>SPECspeed®2017_fp_peak (123)</th>
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<td>180</td>
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<tr>
<td>607.cactuBSSN_s 52</td>
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<td>619.lbm_s 52</td>
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<td>621.wrf_s 52</td>
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<td>627.cam4_s 52</td>
<td>95.6</td>
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<tr>
<td>628.pop2_s 52</td>
<td>60.8</td>
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<tr>
<td>638.imagick_s 52</td>
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<td>644.nab_s 52</td>
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SPECspeed®2017_fp_base = 122
SPECspeed®2017_fp_peak = 123

Results Table

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<th>Ratio</th>
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<td>113</td>
<td>139</td>
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</tr>
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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

SPECspeed\textsuperscript{2017\_fp\_base} = 122
SPECspeed\textsuperscript{2017\_fp\_peak} = 123

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General Notes (Continued)

generally available. At the time of this publication, it may
not be shipping, and/or may not be supported, and/or may fail
to meet other tests of General Availability described in the
SPEC OSG Policy document, \url{http://www.spec.org/osg/policy.html}

This measured result may not be representative of the result
that would be measured were this benchmark run with hardware
and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-nvug Sat Dec 16 01:20:30 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
\url{https://www.spec.org/cpu2017/Docs/config.html#sysinfo}

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Platinum 8170 CPU @ 2.10GHz
- 2 "physical id"s (chips)
- 52 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following
  excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 26
- siblings  : 26
- physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
- physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 52
- On-line CPU(s) list: 0-51
- Thread(s) per core: 1

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

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SPECspeed®2017_fp_peak = 123

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8170 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 2004.779
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4190.13
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-25
NUMA node1 CPU(s): 26-51

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpref perfmonfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pni dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erva invpcid rtm cqm mxpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/platforminfo cache data
  cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
  node 0 size: 192089 MB
  node 0 free: 191262 MB
  node 1 cpus: 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
  node 1 size: 193518 MB
  node 1 free: 192889 MB
  node distances:
    node 0: 10 21
    node 1: 21 10

(Continued on next page)
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SPECspeed®2017_fp_base = 122
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Platform Notes (Continued)

From /proc/meminfo
MemTotal:       394863312 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
   SUSE Linux Enterprise Server 12 (x86_64)
   VERSION = 12
   PATCHLEVEL = 2
   # This file is deprecated and will be removed in a future service pack or release.
   # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-nvug 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 16 04:21

SPEC is set to: /home/cpu2017

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
   24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)

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<td>icc (ICC) 18.0.0 20170811</td>
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<td>Copyright (C) 1985-2017 Intel Corporation. All rights reserved.</td>
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Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

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Base Compiler Invocation (Continued)
Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.ibm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte
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### Base Other Flags

C benchmarks:
- `m64 -std=c11`

Fortran benchmarks:
- `m64`

Benchmarks using both Fortran and C:
- `m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `m64 -std=c11`

### Peak Compiler Invocation

C benchmarks:
- `icc`

Fortran benchmarks:
- `ifort`

Benchmarks using both Fortran and C:
- `ifort icc`

Benchmarks using Fortran, C, and C++:
- `icpc icc ifort`

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:

```bash
619_lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP
```

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**Peak Optimization Flags (Continued)**

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC.Suppress_OPENMP

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -DSPEC.Suppress_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

**Peak Other Flags**

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8170, 2.10 GHz)  

SPECspeed\textsuperscript{®}2017\textsubscript{fp}\textsubscript{peak} = 123
SPECspeed\textsuperscript{®}2017\textsubscript{fp}\textsubscript{base} = 122

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The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU\textsuperscript{®}2017 v1.0.2 on 2017-12-16 04:20:29-0500.
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