# SPEC CPU®2017 Integer Speed Result

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.02</td>
<td>9.29</td>
</tr>
</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Platinum 8168</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal</td>
<td>2700</td>
</tr>
<tr>
<td>Enabled</td>
<td>96 cores, 4 chips</td>
</tr>
<tr>
<td>Orderable</td>
<td>2.4 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>33 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 1 TB SAS HDD, 7.2K RPM</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 12 SP2 (x86_64)</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>Yes</td>
</tr>
<tr>
<td>Firmware</td>
<td>Version 3.1.0 released May-2017</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 5 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other</td>
<td>jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases</td>
</tr>
<tr>
<td>Power Management</td>
<td>--</td>
</tr>
</tbody>
</table>

### Test Details

<table>
<thead>
<tr>
<th>License</th>
<th>CPU2017 License: 9019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Dec-2017</td>
</tr>
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<td>Hardware Availability</td>
<td>Aug-2017</td>
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### Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECspeed®2017_int_base</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>96</td>
<td>7.44</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>96</td>
<td>9.55</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>96</td>
<td>11.0</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>96</td>
<td>7.22</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>96</td>
<td>9.26</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>96</td>
<td>11.9</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>96</td>
<td>13.4</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>96</td>
<td>13.4</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>96</td>
<td>23.6</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>96</td>
<td>23.9</td>
</tr>
</tbody>
</table>

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**Notes:**

- SPEC CPU®2017 is a benchmark suite that evaluates a computer system’s performance for specific tasks.
- The results are based on the performance of the system under test when executing a set of standardized benchmarks.
- The benchmarks used in this test include perlbench, gcc, mcf, omnetpp, xalancbmk, x264, deepsjeng, leela, exchange2, and xz.
- The performance is measured in terms of SPECspeed®, a normalized score that reflects the system's ability to execute the specified benchmarks.
- The SPEC CPU®2017 suite is designed to provide a comprehensive evaluation of the system’s performance across a range of applications.
Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32;/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32;/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3 > /proc/sys/vm/drop_caches
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly (Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

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<td>Software Availability:</td>
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General Notes (Continued)

generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

<table>
<thead>
<tr>
<th>BIOS Settings:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel HyperThreading Technology set to Disabled</td>
</tr>
<tr>
<td>CPU performance set to Enterprise</td>
</tr>
<tr>
<td>Power Performance Tuning set to OS Controls</td>
</tr>
<tr>
<td>SNC set to Disabled</td>
</tr>
<tr>
<td>Patrol Scrub set to Disabled</td>
</tr>
</tbody>
</table>

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-g4f1 Sat Dec 16 03:45:21 2017

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8168 CPU @ 2.70GHz
4 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 1

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)

SPEC CPU®2017 Integer Speed Result

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Tested by: Cisco Systems

SPECspeed®2017_int_base = 9.02
SPECspeed®2017_int_peak = 9.29

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

Core(s) per socket: 24
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8168 CPU @ 2.70GHz
Stepping: 4
CPU MHz: 2263.095
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5400.22
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 33792K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
NUMA node2 CPU(s): 48-71
NUMA node3 CPU(s): 72-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl pge mce cx8 apic
perfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave f16c rdrand lahf_lm abm 3dnowprefetch ida arat eab pni dtherm hw
hp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmmx flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rdtcm qm pxr axv512f
axv512dq rdseed adx smap clflushopt clwb axv512cd axv512bw axv512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occult_llc

/proc/cpuinfo cache data
cache size: 33792 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 192014 MB
node 0 free: 191175 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 193521 MB
node 1 free: 192803 MB
node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 2 size: 193521 MB
node 2 free: 192989 MB

(Continued on next page)
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Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)  

SPECspeed®2017_int_base = 9.02  
SPECspeed®2017_int_peak = 9.29

Platform Notes (Continued)

node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 193372 MB
node 3 free: 192832 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

From /proc/meminfo
MemTotal: 790968404 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME=cpe:/o:suse:sles:12:sp2

uname -a:
Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Jan 15 00:25

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda6 xfs 871G 253G 618G 30% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are (Continued on next page)
SPEC CPU®2017 Integer Speed Result

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SPECspeed®2017_int_base = 9.02
SPECspeed®2017_int_peak = 9.29

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

C
| 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

C++
| 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Fortran
| 648.exchange2_s(base, peak)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
iccc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)

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CPU2017 License: 9019
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Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
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Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags
C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64
# Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8168, 2.70 GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

## Peak Compiler Invocation

C benchmarks:
- icc

C++ benchmarks:
- icpc

Fortran benchmarks:
- ifort

## Peak Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlb benchmark</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
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<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Peak Optimization Flags

### C benchmarks:

- 600.perlb benchmark:  
  -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
  -xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
  -no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
  -DSPEC_OPENMP -fno-strict-overflow  
  -L/usr/local/je5.0.1-64/lib -ljemalloc

- 602.gcc_s:  
  -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
  -xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
  -no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
  -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

- 605.mcf_s:  
  -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
  -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP  
  -L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
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| Test Sponsor | Cisco Systems | Hardware Availability | Aug-2017 |
| Test Date | Dec-2017 | Software Availability | Sep-2017 |
| Tested by | Cisco Systems | |

### SPECspeed®2017_int_base = 9.02

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### Peak Optimization Flags (Continued)

- **625.x264_s**: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc`

- **657.xz_s**: Same as 602.gcc_s

### C++ benchmarks:

- **620.omnetpp_s**: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc`


- **631.deepsjeng_s**: Same as 620.omnetpp_s

- **641.leela_s**: Same as 620.omnetpp_s

### Fortran benchmarks:

- **623.xalancbmk_s**: `-m32`

### Peak Other Flags

- **C benchmarks**: `-m64 -std=c11`

- **C++ benchmarks (except as noted below)**: `-m64`

- **623.xalancbmk_s**: `-m32`

- **Fortran benchmarks**: `-m64`
# SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

```markdown
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```

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The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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