Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

| SPECrate®2017_int_base = 45.5 |
| SPECrate®2017_int_peak = 46.6 |

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Bronze 3106</td>
<td>OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)</td>
</tr>
<tr>
<td>Max MHz: 1700</td>
<td>4.4.21-69-default</td>
</tr>
<tr>
<td>Nominal: 1700</td>
<td>Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Enabled: 16 cores, 2 chips</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Orderable: 1.2 Chips</td>
<td>Firmware: Version 3.2.1d released Jul-2017</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L3: 11 MB I+D on chip per chip</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2133)</td>
<td>Other: jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases</td>
</tr>
<tr>
<td>Storage: 1 x 600 GB SAS HDD, 10K RPM</td>
<td>Power Management: --</td>
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</table>

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
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<tbody>
<tr>
<td>CPU2017 License: 9019</td>
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<td>Test Date: Dec-2017</td>
<td>Hardware Availability: Aug-2017</td>
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<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2017</td>
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<table>
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<tr>
<th>SPEC 2017 Integer Rate Result</th>
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<th>502.gcc_r</th>
<th>505.mcf_r</th>
<th>520.omnetpp_r</th>
<th>523.xalancbmk_r</th>
<th>525.x264_r</th>
<th>531.deepsjeng_r</th>
<th>541.leela_r</th>
<th>548.exchange2_r</th>
<th>557.xz_r</th>
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<td></td>
<td>0 4.00 8.00 12.0 16.0 20.0 24.0 28.0 32.0 36.0 40.0 44.0 48.0 52.0 56.0 60.0 64.0 68.0 72.0 76.0 80.0 84.0 88.0 92.0 96.0</td>
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SPEC 2017 Integer Rate Result

| 40.0 | 44.0 | 48.0 | 52.0 | 56.0 | 60.0 | 64.0 | 68.0 | 72.0 | 76.0 | 80.0 | 84.0 | 88.0 | 92.0 | 96.0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)  

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

Results Table

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<td>579</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

csync; echo 3>/proc/sys/vm/drop_caches

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

| SPECrate®2017_int_base = 45.5 |
| SPECrate®2017_int_peak = 46.6 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux Sat Dec 16 08:46:38 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3106 CPU @ 1.70GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

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<thead>
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<th>SPECrate®2017_int_base</th>
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<td>SPECrate®2017_int_peak</td>
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</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3106 CPU @ 1.70GHz
Stepping: 4
CPU MHz: 1582.672
CPU max MHz: 1700.0000
CPU min MHz: 800.0000
BogoMIPS: 3399.98
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmpref perfok pni pclmulqdq dtes64monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64eguard smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb pni pclmulqdq dtes64guard

/proc/cpuinfo cache data
  cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 191913 MB
node 0 free: 188412 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 193504 MB
node 1 free: 189552 MB
node distances:
node   0   1
0:  10  21

(Continued on next page)
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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_int_base = 45.5
SPECrate®2017_int_peak = 46.6

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

1: 21 10

From /proc/meminfo
MemTotal: 394667604 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67) x86_64
  x86_64 x86_64 GNU/Linux

run-level 3 Jan 2 13:39

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 144G 136G 52% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMI BIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
  Memory:
    24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2133

(End of data from sysinfo program)
Cisco Systems
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SPECrater®2017_int_base = 45.5
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Compiler Version Notes

==============================================================================
<p>| C       | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak) |
|---------------------------------------------------------------|
| icc (ICC) 18.0.0 20170811                                     |</p>
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<td>Fortran</td>
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<td>ifort (IFORT) 18.0.0 20170811</td>
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<td>Copyright (C) 1985-2017 Intel Corporation. All rights reserved.</td>
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Base Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)  

SPECrate®2017_int_base = 45.5
SPECrate®2017_int_peak = 46.6

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Dec-2017  
Hardware Availability: Aug-2017  
Software Availability: Sep-2017

Base Portability Flags (Continued)

541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
  -L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
- m64 -std=c11

C++ benchmarks:
- m64

Fortran benchmarks:
- m64

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort
Cisco Systems
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Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbmk_r: -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3

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## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3106, 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>45.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>46.6</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Sep-2017

## Peak Optimization Flags (Continued)

523.xalancbmk_r (continued):
- `-L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
- `-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`  
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

## Peak Other Flags

C benchmarks (except as noted below):
- `-m64 -std=c11`

502.gcc_r: `-m32 -std=c11`

C++ benchmarks (except as noted below):
- `-m64`

523.xalancbmk_r: `-m32`

Fortran benchmarks:
- `-m64`

The flags files that were used to format this result can be browsed at:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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