# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

### SPECrate®2017_int_base = 109

### SPECrate®2017_int_peak = 114

<table>
<thead>
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<th>Copy</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>80.4</td>
<td>114</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96.1</td>
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</tr>
<tr>
<td>505.mcf_r</td>
<td>63.8</td>
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<tr>
<td>520.omnetpp_r</td>
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<td>523.xalancbmk_r</td>
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<td>525.x264_r</td>
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<tr>
<td>541.leela_r</td>
<td>87.2</td>
<td>88.6</td>
</tr>
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<td>548.exchange2_r</td>
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</tr>
<tr>
<td>557.xz_r</td>
<td>77.0</td>
<td>77.0</td>
</tr>
</tbody>
</table>

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### Hardware

**CPU Name:** Intel Xeon Gold 6134M  
**Max MHz:** 3700  
**Nominal:** 3200  
**Enabled:** 16 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 24.75 MB I+D on chip per chip  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)  
**Storage:** 1 x 600 GB SAS HDD, 10K RPM  
**Other:** None

### Software

**OS:**  
SUSE Linux Enterprise Server 12 SP2 (x86_64)  
4.4.21-69-default

**Compiler:**  
C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;  
Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux

**Parallel:** No

**Firmware:**  
Version 3.2.1d released Jul-2017

**File System:** xfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** 32/64-bit

**Other:**  
jemalloc: jemalloc memory allocator library V5.0.1;  
jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets;  
jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5;  
jemalloc: sources available from jemalloc.net or releases

**Power Management:** --
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>488</td>
<td>70.8</td>
<td>487</td>
<td>71.0</td>
</tr>
</tbody>
</table>

### Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

```plaintext
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```plaintext
sync; echo 3 > /proc/sys/vm/drop_caches
```

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

General Notes (Continued)

past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux Thu Dec 21 18:45:52 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6134M CPU @ 3.20GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPEC CPU®2017 Integer Rate Result
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Sep-2017

SPECrate®2017_int_base = 109
SPECrate®2017_int_peak = 114

Platform Notes (Continued)

CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6134M CPU @ 3.20GHz
Stepping: 4
CPU MHz: 2902.615
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 6399.96
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tcb
aperfmpref eagerfpui pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpx pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsae avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_kpg_req intel_pt tpr_shadow vmvi flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Platform Notes (Continued)**

```
0:  10  21
1:  21  10
```

From `/proc/meminfo`

- MemTotal: 395441684 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`

- SuSE-release:
  - VERSION = 12
  - PATCHLEVEL = 2
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check `/etc/os-release` for details about this release.
- os-release:
  - NAME="SLES"
  - VERSION="12-SP2"
  - VERSION_ID="12.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  - ID="sles"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:12:sp2"

```
uname -a:
Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67) x86_64 x86_64 GNU/Linux
```

run-level 3 Jan 2 17:25

SPEC is set to: /home/cpu2017

```
Filesystem  Type  Size  Used  Avail  Use% Mounted on
/dev/sda1   xfs   280G  146G  134G  53% /
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
- Memory:
  - 24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPEC CPU®2017 Integer Rate Result
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Test Date: Dec-2017
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Software Availability: Sep-2017

Compiler Version Notes
==============================================================================
C       | 500.perlb ench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbm k_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbm k_r: -DSPEC_LP64 -DSPEC LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64

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Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

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<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
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<table>
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<tr>
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<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
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### Base Portability Flags (Continued)

541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

**Fortran benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
- -L/usr/local/je5.0.1-64/lib -ljemalloc

### Base Other Flags

**C benchmarks:**
- -m64 -std=c11

**C++ benchmarks:**
- -m64

**Fortran benchmarks:**
- -m64

### Peak Compiler Invocation

**C benchmarks:**
- icc

**C++ benchmarks:**
- icpc

**Fortran benchmarks:**
- ifort
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

| SPECrate®2017_int_base | 109 |
| SPECrate®2017_int_peak | 114 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

### Peak Portability Flags

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<th>Benchmark</th>
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<td>perlbench_r</td>
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</tr>
<tr>
<td>gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<tr>
<td>mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>depsjeng_r</td>
<td>-DSPEC_LP64</td>
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<td>leela_r</td>
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<td>exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xz_r</td>
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### Peak Optimization Flags

#### C benchmarks:

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<tr>
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<tbody>
<tr>
<td>perlbench_r</td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
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<tr>
<td></td>
<td>-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3</td>
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<tr>
<td></td>
<td>-fno-strict-overflow -L/usr/local/je5.0.1-64/lib</td>
</tr>
<tr>
<td></td>
<td>-ljemalloc</td>
</tr>
<tr>
<td>gcc_r</td>
<td>-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32</td>
</tr>
<tr>
<td></td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
</tr>
<tr>
<td></td>
<td>-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3</td>
</tr>
<tr>
<td></td>
<td>-L/usr/local/je5.0.1-32/lib -ljemalloc</td>
</tr>
<tr>
<td>mcf_r</td>
<td>-Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div</td>
</tr>
<tr>
<td></td>
<td>-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib</td>
</tr>
<tr>
<td></td>
<td>-ljemalloc</td>
</tr>
<tr>
<td>x264_r</td>
<td>-Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div</td>
</tr>
<tr>
<td></td>
<td>-qopt-mem-layout-trans=3 -fno-alias</td>
</tr>
<tr>
<td></td>
<td>-L/usr/local/je5.0.1-64/lib -ljemalloc</td>
</tr>
<tr>
<td>xz_r</td>
<td>Same as 505.mcf_r</td>
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#### C++ benchmarks:

<table>
<thead>
<tr>
<th>Benchmark</th>
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</tr>
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<tbody>
<tr>
<td>omnetpp_r</td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
</tr>
<tr>
<td></td>
<td>-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3</td>
</tr>
<tr>
<td></td>
<td>-L/usr/local/je5.0.1-64/lib -ljemalloc</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>-L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32</td>
</tr>
<tr>
<td></td>
<td>-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo</td>
</tr>
<tr>
<td></td>
<td>-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3</td>
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(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPEC CPU®2017 Integer Rate Result

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SPECrate®2017_int_base = 109
SPECrate®2017_int_peak = 114

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Optimization Flags (Continued)

523.xalancbmk_r (continued):
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r
541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11
502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64
523.xalancbmk_r: -m32

Fortran benchmarks:
-m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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