# Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>192</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>191</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Dec-2017  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Tested by:** Cisco Systems  
**Software Availability:** Sep-2017

## Threads

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>99-112</td>
<td>266</td>
<td>274</td>
</tr>
<tr>
<td>122</td>
<td></td>
<td></td>
</tr>
<tr>
<td>132</td>
<td></td>
<td></td>
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<tr>
<td>142</td>
<td></td>
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<tr>
<td>152</td>
<td></td>
<td></td>
</tr>
<tr>
<td>162</td>
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<td></td>
</tr>
<tr>
<td>172</td>
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<tr>
<td>182</td>
<td></td>
<td></td>
</tr>
<tr>
<td>192</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Hardware

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Platinum 8180M</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3800</td>
</tr>
<tr>
<td>Nominal</td>
<td>2500</td>
</tr>
<tr>
<td>Enabled</td>
<td>112 cores, 4 chips</td>
</tr>
<tr>
<td>Orderable</td>
<td>2.4 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>38.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 1 TB SAS HDD, 7.2K RPM</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

## Software

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>Yes</td>
</tr>
<tr>
<td>Firmware</td>
<td>Version 3.1.0 released May-2017</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 5 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Power Management</td>
<td>--</td>
</tr>
</tbody>
</table>
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>112</td>
<td>74.7</td>
<td></td>
<td>73.6</td>
<td>802</td>
<td></td>
<td>74.0</td>
<td>797</td>
<td></td>
<td>73.5</td>
<td>803</td>
<td></td>
<td>77.4</td>
<td>762</td>
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</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>112</td>
<td>62.6</td>
<td>266</td>
<td>62.5</td>
<td>267</td>
<td>266</td>
<td>62.6</td>
<td>266</td>
<td>60.6</td>
<td>275</td>
<td>60.9</td>
<td>274</td>
<td>60.9</td>
<td>274</td>
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<tr>
<td>619.ibm_s</td>
<td>112</td>
<td>61.9</td>
<td>84.6</td>
<td>65.4</td>
<td>80.1</td>
<td>62.0</td>
<td>84.5</td>
<td></td>
<td></td>
<td>62.1</td>
<td>84.4</td>
<td>62.2</td>
<td>84.2</td>
<td></td>
<td></td>
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<tr>
<td>621.wrf_s</td>
<td>112</td>
<td>161</td>
<td>82.1</td>
<td>161</td>
<td>82.3</td>
<td>164</td>
<td>80.8</td>
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<td>627.cam4_s</td>
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<td>53.7</td>
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<td>54.1</td>
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<td>53.6</td>
<td>165</td>
<td>54.0</td>
<td>164</td>
<td>53.9</td>
<td>164</td>
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<td>628.pop2_s</td>
<td>112</td>
<td>187</td>
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<td>194</td>
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<td>63.3</td>
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<td>638.imagick_s</td>
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<td>257</td>
<td>55.2</td>
<td>261</td>
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<td>265</td>
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<td>644.nab_s</td>
<td>112</td>
<td>37.1</td>
<td>471</td>
<td>37.1</td>
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<td>37.0</td>
<td>472</td>
<td>37.0</td>
<td>472</td>
<td>37.0</td>
<td>472</td>
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<tr>
<td>649.fotonik3d_s</td>
<td>112</td>
<td>77.6</td>
<td>117</td>
<td>78.5</td>
<td>116</td>
<td>76.7</td>
<td>119</td>
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<td>119</td>
<td>81.5</td>
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<td>84.2</td>
<td>108</td>
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<tr>
<td>654.roms_s</td>
<td>112</td>
<td>50.9</td>
<td>310</td>
<td>49.5</td>
<td>318</td>
<td>53.6</td>
<td>294</td>
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<td></td>
<td>50.8</td>
<td>310</td>
<td>52.7</td>
<td>299</td>
<td>52.8</td>
<td>298</td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 192
SPECspeed®2017_fp_peak = 191

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3 > /proc/sys/vm/drop_caches`

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed®2017_fp_base = 192
SPECspeed®2017_fp_peak = 191

Platform Notes (Continued)

running on linux-g4f1 Fri Dec  8 11:56:20 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Platinum 8180M CPU @ 2.50GHz
  4 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                112
On-line CPU(s) list:   0-111
Thread(s) per core:    1
Core(s) per socket:    28
Socket(s):             4
NUMA node(s):          4
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Platinum 8180M CPU @ 2.50GHz
Stepping:              4
CPU MHz:               1317.387
CPU max MHz:           3800.0000
CPU min MHz:           1000.0000
BogoMIPS:              5000.18
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              39424K

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

NUMA node0 CPU(s): 0-27
NUMA node1 CPU(s): 28-55
NUMA node2 CPU(s): 56-83
NUMA node3 CPU(s): 84-111
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 collapse dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch idap ebp pln pts dtherm hw lp_act_window hwlp pkg_req intel_pt tpr_shadow vmm flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow ermsi invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data
  cache size : 39424 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  node 0 size: 192014 MB
  node 0 free: 190164 MB
  node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
  node 1 size: 193521 MB
  node 1 free: 190567 MB
  node 2 cpus: 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83
  node 2 size: 193521 MB
  node 2 free: 191878 MB
  node 3 cpus: 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111
  node 3 size: 193372 MB
  node 3 free: 190541 MB
  node distances:
  node 0 1 2 3
  0: 10 21 21 21
  1: 21 10 21 21
  2: 21 21 10 21
  3: 21 21 21 10

From /proc/meminfo
  MemTotal: 790968344 KB
  HugePages_Total: 0
  Hugepagesize: 2048 KB

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed®2017_fp_base = 192
SPECspeed®2017_fp_peak = 191

Platform Notes (Continued)

/usr/bin/lsb_release -d
    SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
    os-release:
        NAME="SLES"
        VERSION="12-SP2"
        VERSION_ID="12.2"
        PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
        ID="sles"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Jan 6 21:15

SPEC is set to: /home/cpu2017
    Filesystem     Type  Size  Used Avail Use% Mounted on
    /dev/sda6      xfs   871G  253G  618G  30% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

    BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
    Memory:
        48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C          | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
           | 644.nab_s(base, peak)
==============================================================================

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECsustainability® 2017 fp_base = 192
SPECsustainability® 2017 fp_peak = 191

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
==============================================================================

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
==============================================================================

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
==============================================================================

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

| SPECspeed®2017_fp_base = 192 |
| SPECspeed®2017_fp_peak = 191 |

CPU2017 License: 9019
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Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
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Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

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Base Other Flags (Continued)

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

SPECspeed\textsuperscript{®}2017\_fp\_peak = 191

SPECSpeed\textsuperscript{®}2017\_fp\_base = 192

CPU2017 License: 9019
Test Date: Dec-2017
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Optimization Flags (Continued)

Fortran benchmarks:
-\texttt{-prof-gen(pass 1) -prof-use(pass 2) -DSPEC\_SUPPRESS\_OPENMP}
-\texttt{-DSPEC\_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3}
-\texttt{-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp}
-\texttt{-nostandard-realloc-lhs -align array32byte}

Benchmarks using both Fortran and C:

\texttt{621.wrf\_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512}
\texttt{-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div}
\texttt{-qopt-mem-layout-trans=3 -DSPEC\_SUPPRESS\_OPENMP -qopenmp}
\texttt{-DSPEC\_OPENMP -nostandard-realloc-lhs -align array32byte}

\texttt{627.cam4\_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch}
\texttt{-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp}
\texttt{-DSPEC\_OPENMP -nostandard-realloc-lhs -align array32byte}

\texttt{628.pop2\_s: Same as 621.wrf\_s}

Benchmarks using Fortran, C, and C++:
-\texttt{-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch}
-\texttt{-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3}
-\texttt{-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP -nostandard-realloc-lhs}
-\texttt{-align array32byte}

Peak Other Flags

C benchmarks:
-\texttt{-m64 -std=c11}

Fortran benchmarks:
-\texttt{-m64}

Benchmarks using both Fortran and C:
-\texttt{-m64 -std=c11}

Benchmarks using Fortran, C, and C++:
-\texttt{-m64 -std=c11}

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8180M, 2.50 GHz)

<table>
<thead>
<tr>
<th>SPECspeed²017 fp_base = 192</th>
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<tbody>
<tr>
<td>SPECspeed²017 fp_peak = 191</td>
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</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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