Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4112, 2.60 GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 44.0</th>
<th>SPECrate®2017_int_peak = 46.9</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Dec-2017</td>
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<td>Aug-2017</td>
</tr>
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</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>40.6</td>
<td>46.9</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>39.7</td>
<td>54.2</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>28.0</td>
<td>38.5</td>
</tr>
<tr>
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<td>56.9</td>
</tr>
<tr>
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<td>84.5</td>
<td>88.5</td>
</tr>
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<td>37.4</td>
<td>81.9</td>
</tr>
<tr>
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<td>37.5</td>
<td>81.8</td>
</tr>
<tr>
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<td>35.1</td>
<td>81.8</td>
</tr>
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</tr>
<tr>
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<td>32.1</td>
<td>32.1</td>
</tr>
</tbody>
</table>

### Hardware

**CPU Name:** Intel Xeon Silver 4112  
**Max MHz:** 3000  
**Nominal:** 2600  
**Enabled:** 8 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 8.25 MB I+D on chip per chip  
**Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)  
**Storage:** 1 x 600 GB SAS HDD, 10K RPM  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)  
**Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux  
**Parallel:** No  
**Firmware:** Version 3.1.1d released Jun-2017  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc: jemalloc memory allocator library V5.0.1; jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets; jemalloc: built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5; jemalloc: sources available from jemalloc.net or releases  
**Power Management:** --
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SPEC CPU®2017 Integer Rate Result
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>16</td>
<td>784</td>
<td>32.5</td>
<td>788</td>
<td>32.3</td>
<td>792</td>
<td>32.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>16</td>
<td>570</td>
<td>39.7</td>
<td>569</td>
<td>39.8</td>
<td>571</td>
<td>39.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>16</td>
<td>477</td>
<td>54.2</td>
<td>477</td>
<td>54.2</td>
<td>457</td>
<td>56.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>16</td>
<td>753</td>
<td>27.9</td>
<td>749</td>
<td>28.0</td>
<td>750</td>
<td>28.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>16</td>
<td>350</td>
<td>48.3</td>
<td>347</td>
<td>48.6</td>
<td>348</td>
<td>48.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>16</td>
<td>332</td>
<td>84.5</td>
<td>332</td>
<td>84.5</td>
<td>328</td>
<td>85.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>16</td>
<td>490</td>
<td>37.4</td>
<td>491</td>
<td>37.4</td>
<td>491</td>
<td>37.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>16</td>
<td>760</td>
<td>34.9</td>
<td>762</td>
<td>34.8</td>
<td>763</td>
<td>34.7</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>16</td>
<td>513</td>
<td>81.8</td>
<td>512</td>
<td>81.9</td>
<td>512</td>
<td>81.9</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>16</td>
<td>539</td>
<td>32.1</td>
<td>539</td>
<td>32.1</td>
<td>538</td>
<td>32.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Submit Notes
The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-a0tk Tue Dec 5 19:17:03 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 8
physical 0: cores 1 2 4 5
physical 1: cores 0 1 3 4

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 2
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4112 CPU @ 2.60GHz
Stepping: 4
CPU MHz: 2824.338
CPU max MHz: 3000.0000
CPU min MHZ: 800.0000
BogoMIPS: 5187.84
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K

(Continued on next page)
Platform Notes (Continued)

NUMA node0 CPU(s): 0-3,8-11
NUMA node1 CPU(s): 4-7,12-15
Flags: fpu vme de pse tsc msr pae mca cmov
       pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl mce cx8 apic sep mtrr pge mca
       cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl mce cx8 apic sep mtrr pge mca
       cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl mce cx8 apic sep mtrr pge mca
       cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
       lm constant_tsc art arch_perfmon pebs bts rep_good nopl mce cx8 apic sep mtrr pge mca
       cmov

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 8 9 10 11
   node 0 size: 192090 MB
   node 0 free: 187852 MB
   node 1 cpus: 4 5 6 7 12 13 14 15
   node 1 size: 193518 MB
   node 1 free: 190282 MB
   node distances:
   node   0   1
   0: 10 21
   1: 21 10

From /proc/meminfo
   MemTotal: 394863492 kB
   HugePages_Total: 0
   Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 2
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"

(Continued on next page)
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Platform Notes (Continued)

VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-a0tk 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 5 04:58
SPEC is set to: /home/cpu2017

Filesystem      Type Size  Used Avail Use% Mounted on
/dev/sda7       xfs  416G  119G  298G  29% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
    Memory:
        24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
|      | 500.perlbench_r(base, peak) | 502.gcc_r(base, peak) | 505.mcf_r(base, peak) | 525.x264_r(base, peak) | 557.xz_r(base, peak) |
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------
|      | 520.omnetpp_r(base, peak) | 523.xalancbmk_r(base, peak) | 525.xz_r(base, peak) | 531.deepsjeng_r(base, peak) | 541.leela_r(base, peak) |
-----------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------

(Continued on next page)
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SPECratenet.org 2017 Integer Rate Result
SPECratenet.org 2017 int_base = 44.0
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Compiler Version Notes (Continued)

Fortran | 548.exchange2_r (base, peak)
------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc
C++ benchmarks:
icpc
Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Base Optimization Flags (Continued)
Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags
C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Peak Compiler Invocation
C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
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Peak Optimization Flags

C benchmarks:

500.perlbench_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/usr/local/je5.0.1-64/lib
-ljemalloc

502.gcc_r -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib
-ljemalloc

525.x264_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/usr/local/je5.0.1-64/lib -ljemalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-64/lib -ljemalloc

523.xalancbk_r -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=3
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
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Peak Other Flags

C benchmarks (except as noted below):
-m64 -std=c11
502.gcc_r: -m32 -std=c11

C++ benchmarks (except as noted below):
-m64
523.xalancbmk_r: -m32

Fortran benchmarks:
-m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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