Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

<table>
<thead>
<tr>
<th>Copy</th>
<th>503.bwaves_r</th>
<th>507.cactuBSSN_r</th>
<th>508.namd_r</th>
<th>510.parest_r</th>
<th>511.povray_r</th>
<th>519.lbm_r</th>
<th>521.wrf_r</th>
<th>526.blender_r</th>
<th>527.cam4_r</th>
<th>538.imagick_r</th>
<th>544.nab_r</th>
<th>549.fotonik3d_r</th>
<th>554.roms_r</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>105</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>120</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>135</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>150</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>165</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>180</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>195</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>210</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>225</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>240</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>255</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>270</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>285</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>315</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>330</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Hardware**

- **CPU Name:** Intel Xeon Silver 4110
- **Max MHz:** 3000
- **Nominal:** 2100
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM
- **Other:** None

---

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **4.4.21-69-default**
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 3.2.1d released Jul-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>32</td>
<td>984</td>
<td>326</td>
<td>982</td>
<td>327</td>
<td>984</td>
<td>326</td>
<td>983</td>
<td>327</td>
<td>982</td>
<td>327</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>32</td>
<td>579</td>
<td>69.9</td>
<td>579</td>
<td>70.0</td>
<td>579</td>
<td>70.0</td>
<td>591</td>
<td>68.5</td>
<td>593</td>
<td>68.4</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>32</td>
<td>548</td>
<td>55.5</td>
<td>548</td>
<td>55.4</td>
<td>547</td>
<td>55.6</td>
<td>547</td>
<td>55.6</td>
<td>544</td>
<td>55.8</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>32</td>
<td>1403</td>
<td>59.7</td>
<td>1406</td>
<td>59.6</td>
<td>1411</td>
<td>59.3</td>
<td>1406</td>
<td>59.5</td>
<td>1401</td>
<td>59.8</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>32</td>
<td>829</td>
<td>90.1</td>
<td>829</td>
<td>90.4</td>
<td>824</td>
<td>90.6</td>
<td>718</td>
<td>104</td>
<td>709</td>
<td>105</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>32</td>
<td>492</td>
<td>68.5</td>
<td>490</td>
<td>68.8</td>
<td>491</td>
<td>68.7</td>
<td>432</td>
<td>78.1</td>
<td>435</td>
<td>77.6</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>32</td>
<td>803</td>
<td>89.2</td>
<td>807</td>
<td>88.9</td>
<td>799</td>
<td>89.7</td>
<td>770</td>
<td>93.1</td>
<td>781</td>
<td>91.8</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>32</td>
<td>637</td>
<td>76.5</td>
<td>634</td>
<td>76.9</td>
<td>634</td>
<td>76.8</td>
<td>633</td>
<td>77.0</td>
<td>633</td>
<td>77.0</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>32</td>
<td>855</td>
<td>65.4</td>
<td>853</td>
<td>65.6</td>
<td>853</td>
<td>65.6</td>
<td>841</td>
<td>66.6</td>
<td>839</td>
<td>66.7</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>32</td>
<td>721</td>
<td>110</td>
<td>721</td>
<td>110</td>
<td>721</td>
<td>110</td>
<td>721</td>
<td>110</td>
<td>721</td>
<td>110</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>32</td>
<td>557</td>
<td>96.6</td>
<td>558</td>
<td>96.6</td>
<td>557</td>
<td>96.7</td>
<td>548</td>
<td>98.2</td>
<td>549</td>
<td>98.1</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>32</td>
<td>1310</td>
<td>95.2</td>
<td>1314</td>
<td>94.9</td>
<td>1311</td>
<td>95.1</td>
<td>1309</td>
<td>95.3</td>
<td>1311</td>
<td>95.1</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>32</td>
<td>995</td>
<td>51.1</td>
<td>994</td>
<td>51.1</td>
<td>994</td>
<td>51.2</td>
<td>955</td>
<td>53.3</td>
<td>956</td>
<td>53.2</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/jes.5.0.1-32:/home/cpu2017/jes.5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 84.3
SPECrate®2017_fp_peak = 86.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Sep-2017

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-qc7k Sun Nov 26 00:06:58 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz
Stepping: 4
CPU MHz: 1073.721
CPU max MHz: 3000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

| CPU2017 License: | 9019 |
| Test Sponsor:     | Cisco Systems |
| Tested by:       | Cisco Systems |
| Test Date:       | Nov-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Sep-2017 |

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base** = 84.3

**SPECrate®2017_fp_peak** = 86.8

**Platform Notes (Continued)**

L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mca cmov
        pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
        lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
        aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
        fma cx16 xptr pdcm pcd cda sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
        xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
        hw_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmvi fmaxpriori ept vpid
        fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invpcid rtm cqm mpx avx512f
        avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
        xgetb1 cqm_llc cqm_occup_llc

```
From /proc/cpuinfo cache data
    cache size : 11264 KB
```

```
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
    physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
    node 0 size: 192830 MB
    node 0 free: 192109 MB
    node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
    node 1 size: 193504 MB
    node 1 free: 192835 MB
    node distances:
    node 0 1
      0: 10 21
      1: 21 10
```

```
From /proc/meminfo

    MemTotal: 395606536 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*

    SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
    os-release:
    NAME="SLES"
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPECrate®2017_fp_base = 84.3
SPECrate®2017_fp_peak = 86.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-qc7k 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 31 19:32

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 38G 187G 17% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
==============================================================================

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPECrates

SPECrate®2017_fp_base = 84.3
SPECrate®2017_fp_peak = 86.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Copyright 2017-2020 Standard Performance Evaluation Corporation

Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-------------------------------------------------------------------------------

C++, C, Fortran | 507.cactuBSSN_r(base, peak)
-------------------------------------------------------------------------------

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-------------------------------------------------------------------------------

Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
554.roms_r(base, peak)
-------------------------------------------------------------------------------

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

-------------------------------------------------------------------------------

Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
-------------------------------------------------------------------------------

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)  

SPECrate®2017_fp_base = 84.3
SPECrate®2017_fp_peak = 86.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

**Base Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:
- ifort icc

Benchmarks using both C and C++:
- icpc icc

Benchmarks using Fortran, C, and C++:
- icpc icc ifort

**Base Portability Flags**

- 503.bwaves_r: -DSPEC_LP64
- 507.cactusBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

**C benchmarks:**
- -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3

**C++ benchmarks:**
- -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3

**Fortran benchmarks:**
- -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
- -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPECrates®2017_fp_base = 84.3
SPECrates®2017_fp_peak = 86.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using both C and C++:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

**SPEC CPU®2017 Floating Point Rate Result**

Copyright 2017-2020 Standard Performance Evaluation Corporation

**SPECrate®2017_fp_base = 84.3**

**SPECrate®2017_fp_peak = 86.8**

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2017</td>
</tr>
</tbody>
</table>

**Peak Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:

```plaintext
ifort icc
```

Benchmarks using both C and C++:

```plaintext
icpc icc
```

Benchmarks using Fortran, C, and C++:

```plaintext
icpc icc ifort
```

**Peak Portability Flags**

Same as Base Portability Flags

**Peak Optimization Flags**

C benchmarks:

```plaintext
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r
```

C++ benchmarks:

```plaintext
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```plaintext
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
```

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>84.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>86.8</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Nov-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags (Continued)

554.roms_r (continued):
- align array32byte

Benchmarks using both Fortran and C:
- prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
- no-prec-div -qopt-prefetch -ffinite-math-only  
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
- prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
- no-prec-div -qopt-prefetch -ffinite-math-only  
- qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
- prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
- no-prec-div -qopt-prefetch -ffinite-math-only  
- qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

### Peak Other Flags

**C benchmarks:**
- m64 -std=c11

**C++ benchmarks:**
- m64

**Fortran benchmarks:**
- m64

Benchmarks using both Fortran and C:
- m64 -std=c11

Benchmarks using both C and C++:
- m64 -std=c11

Benchmarks using Fortran, C, and C++:
- m64 -std=c11

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html  
## Cisco Systems

**Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>84.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>86.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Nov-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-11-26 00:06:58-0500.


Originally published on 2017-12-26.