## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Nov-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

### SPECspeed®2017_fp_base = 112

### SPECspeed®2017_fp_peak = 114

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.1d released Jun-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --

### Hardware

- **CPU Name:** Intel Xeon Gold 6142M
- **Max MHz:** 3700
- **Nominal:** 2600
- **Enabled:** 32 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 480 GB SAS SSD
- **Other:** None

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
<td>148</td>
<td>150</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>32</td>
<td>43.5</td>
<td>43.6</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
<td>88.3</td>
<td>91.9</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>32</td>
<td>73.6</td>
<td>73.8</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>32</td>
<td>68.4</td>
<td>68.8</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>32</td>
<td>99.6</td>
<td>99.6</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
<td>80.8</td>
<td>80.8</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>32</td>
<td>191</td>
<td>191</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>32</td>
<td>156</td>
<td>156</td>
</tr>
</tbody>
</table>

---

### Additional Information

- **Testing Sponsor:** Cisco Systems
- **Testing Date:** Nov-2017
- **Hardware Availability:** Aug-2017
- **Software Availability:** Sep-2017
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Nov-2017</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
<td>122</td>
<td>485</td>
<td>121</td>
<td>486</td>
<td>122</td>
<td>485</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>32</td>
<td>112</td>
<td>148</td>
<td>112</td>
<td>148</td>
<td>113</td>
<td>148</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
<td>120</td>
<td>43.5</td>
<td>120</td>
<td>43.5</td>
<td>120</td>
<td>43.5</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>32</td>
<td>149</td>
<td>88.5</td>
<td>150</td>
<td>88.3</td>
<td>145</td>
<td>91.2</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>32</td>
<td>120</td>
<td>73.6</td>
<td>120</td>
<td>73.9</td>
<td>120</td>
<td>73.8</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>32</td>
<td>174</td>
<td>68.3</td>
<td>174</td>
<td>68.4</td>
<td>172</td>
<td>68.6</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
<td>145</td>
<td>99.6</td>
<td>145</td>
<td>99.3</td>
<td>144</td>
<td>98.8</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>32</td>
<td>91.4</td>
<td>191</td>
<td>91.6</td>
<td>191</td>
<td>91.5</td>
<td>191</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
<td>113</td>
<td>80.7</td>
<td>113</td>
<td>80.8</td>
<td>113</td>
<td>80.9</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>32</td>
<td>105</td>
<td>150</td>
<td>105</td>
<td>150</td>
<td>101</td>
<td>156</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base = 112**

**SPECspeed®2017_fp_peak = 114**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

### Platform Notes

BIOS Settings:

- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
## Platform Notes (Continued)

running on linux-79ix Sun Nov 12 10:36:51 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
  2 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                32
On-line CPU(s) list:   0-31
Thread(s) per core:    1
Core(s) per socket:    16
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
Stepping:              4
CPU MHz:               1321.281
CPU max MHz:           3700.0000
CPU min MHz:           1000.0000
BogoMIPS:              5187.80
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              22528K
NUMA node0 CPU(s):     0-15
NUMA node1 CPU(s):     16-31
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu nni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
```

(Continued on next page)
## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 112</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = 114</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>Test Date:</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Nov-2017</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Hardware Availability:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Aug-2017</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tested by:</th>
<th>Software Availability:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

---

### Platform Notes (Continued)

```shell
fma cx16 xtpr pdcm pcid dca dca sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat ebp pln pts dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmmi flexpriority ept vpid fsqsbse tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc
```

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.

```shell
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 192019 MB
node 0 free: 188140 MB
node 0 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 193384 MB
node 1 free: 188902 MB
node distances:
  node  0  1
  0:  10  21
  1:  21  10
```

From `/proc/meminfo`

```shell
MemTotal:       394653864 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From `/etc/*release* /etc/*version*`

```shell
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```shell
uname -a:
Linux linux-79ix 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECspeed®2017_fp_base = 112
SPECspeed®2017_fp_peak = 114

Platform Notes (Continued)

x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Nov 12 05:29

SPEC is set to: /home/cpu2017
Filesysten Type Size Used Avail Use% Mounted on
/dev/sdb7 xfs 416G 81G 336G 20% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)  

| SPECspeed®2017_fp_base = 112 |
| SPECspeed®2017_fp_peak = 114 |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

Test Date: Nov-2017  
Hardware Availability: Aug-2017  
Software Availability: Sep-2017

Compiler Version Notes (Continued)

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)  
                 | 628.pop2_s(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:  
icc

Fortran benchmarks:  
ifort

Benchmarks using both Fortran and C:  
ifort icc

Benchmarks using Fortran, C, and C++:  
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>112</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>114</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  Test Date: Nov-2017
Test Sponsor: Cisco Systems  Hardware Availability: Aug-2017
Tested by: Cisco Systems  Software Availability: Sep-2017

### Base Optimization Flags

C benchmarks:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
- -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
- -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs -align array32byte

### Base Other Flags

C benchmarks:
- -m64 -std=c11

Fortran benchmarks:
- -m64

Benchmarks using both Fortran and C:
- -m64 -std=c11

Benchmarks using Fortran, C, and C++:
- -m64 -std=c11

### Peak Compiler Invocation

C benchmarks:
- icc

Fortran benchmarks:
- ifort

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECspeed®2017_fp_base = 112
SPECspeed®2017_fp_peak = 114

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECspeed®2017_fp_base = 112
SPECspeed®2017_fp_peak = 114

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Optimization Flags (Continued)

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-11-12 13:36:50-0500.
Originally published on 2017-12-09.