



SPEC® CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint®_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019

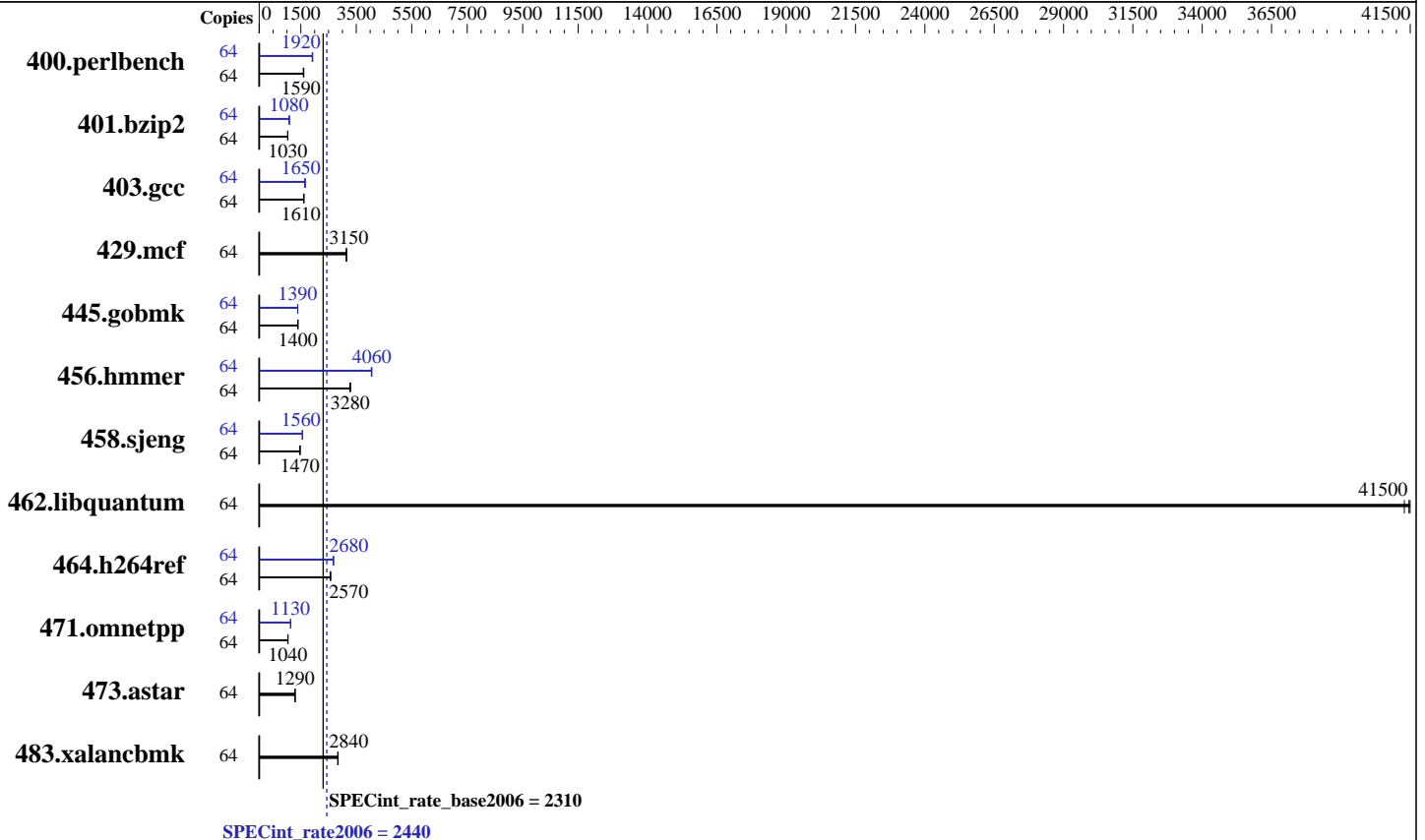
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017



Hardware

CPU Name: Intel Xeon Gold 6144
 CPU Characteristics: Intel Turbo Boost Technology up to 4.20 GHz
 CPU MHz: 3500
 FPU: Integrated
 CPU(s) enabled: 32 cores, 4 chips, 8 cores/chip, 2 threads/core
 CPU(s) orderable: 2,4 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 1 MB I+D on chip per core
 L3 Cache: 24.75 MB I+D on chip per chip
 Other Cache: None
 Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
 Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM
 Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.0.128 of Intel Fortran
 Auto Parallel: Yes
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V10.2



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	64	<u>392</u>	<u>1590</u>	389	1610	392	1590	64	324	1930	327	1910	<u>326</u>	<u>1920</u>
401.bzip2	64	599	1030	<u>599</u>	<u>1030</u>	601	1030	64	570	1080	568	1090	<u>569</u>	<u>1080</u>
403.gcc	64	<u>320</u>	<u>1610</u>	321	1600	319	1610	64	313	1640	310	1660	<u>312</u>	<u>1650</u>
429.mcf	64	185	3150	<u>186</u>	<u>3150</u>	186	3140	64	185	3150	<u>186</u>	<u>3150</u>	186	3140
445.gobmk	64	482	1390	481	1400	<u>481</u>	<u>1400</u>	64	<u>483</u>	<u>1390</u>	483	1390	484	1390
456.hammer	64	<u>182</u>	<u>3280</u>	183	3270	181	3300	64	<u>147</u>	<u>4060</u>	148	4040	147	4060
458.sjeng	64	<u>526</u>	<u>1470</u>	526	1470	526	1470	64	497	1560	497	1560	<u>497</u>	<u>1560</u>
462.libquantum	64	32.0	41500	32.1	41300	<u>32.0</u>	<u>41500</u>	64	32.0	41500	32.1	41300	<u>32.0</u>	<u>41500</u>
464.h264ref	64	554	2560	548	2580	<u>552</u>	<u>2570</u>	64	<u>528</u>	<u>2680</u>	528	2680	532	2660
471.omnetpp	64	<u>386</u>	<u>1040</u>	387	1030	386	1040	64	<u>353</u>	<u>1130</u>	353	1130	353	1130
473.astar	64	348	1290	<u>347</u>	<u>1290</u>	347	1290	64	348	1290	<u>347</u>	<u>1290</u>	347	1290
483.xalancbmk	64	<u>155</u>	<u>2840</u>	155	2850	156	2830	64	<u>155</u>	<u>2840</u>	155	2850	156	2830

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993

Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)

running on linux-qiwr Fri Dec 15 19:32:25 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6144 CPU @ 3.50GHz

Continued on next page

Standard Performance Evaluation Corporation

info@spec.org

<http://www.spec.org/>



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```

4 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27
physical 2: cores 0 2 3 9 16 19 26 27
physical 3: cores 0 2 3 9 16 19 26 27
cache size : 25344 KB

```

```

From /proc/meminfo
MemTotal:      791027744 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

```

uname -a:
Linux linux-qiw 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

```

run-level 3 Dec 15 19:27

```

SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal       xfs   280G   29G  251G  11% /
Additional information from dmidecode:

```

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Platform Notes (Continued)

Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/intel/lib/ia32:/opt/intel/lib/intel64:/opt/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/transparent_hugepage/enabled

Filesystem page cache cleared with:

shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run

runspec command invoked through numactl i.e.:

numactl --interleave=all runspec <etc>

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, <http://www.spec.org/osg/policy.html>

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:

icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32

C++ benchmarks:

icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144,
3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Base Portability Flags

```
400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:

```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
-Wl,-z,muldefs -L/opt/cpu2006-1.2/sh10.2 -lsmartheap
```

Base Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

```
400.perlbench: icc -m64
```

```
401.bzip2: icc -m64
```

```
456.hmmer: icc -m64
```

```
458.sjeng: icc -m64
```

C++ benchmarks:

```
icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3

403.gcc: -xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: -xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto-ilp32
-qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6144, 3.50 GHz)

SPECint_rate2006 = 2440

SPECint_rate_base2006 = 2310

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Peak Optimization Flags (Continued)

C++ benchmarks:

```
471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
             -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2)
             -qopt-ra-region-strategy=block
             -qopt-mem-layout-trans=3 -Wl,-z,muldefs
             -L/opt/cpu2006-1.2/sh10.2 -lsmartheap
```

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Fri Apr 20 19:48:03 2018 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 23 February 2018.