Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPEClnt_rate2006 = 1120
SPEClnt_rate_base2006 = 1060

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Gold 6134M
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 3200
FPU: Integrated
CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: 24.75 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 480 GB SSD SAS
Other Hardware: None

Software
Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPECint_rate2006 = 1120
SPECint_rate_base2006 = 1060

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>32</td>
<td>408</td>
<td>766</td>
<td>408</td>
<td>766</td>
<td>404</td>
<td>773</td>
<td>32</td>
<td>342</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>32</td>
<td>619</td>
<td>499</td>
<td>621</td>
<td>497</td>
<td>623</td>
<td>496</td>
<td>32</td>
<td>586</td>
</tr>
<tr>
<td>403.gcc</td>
<td>32</td>
<td>323</td>
<td>797</td>
<td>323</td>
<td>798</td>
<td>322</td>
<td>799</td>
<td>32</td>
<td>320</td>
</tr>
<tr>
<td>429.mcf</td>
<td>32</td>
<td>185</td>
<td>1580</td>
<td>185</td>
<td>1580</td>
<td>184</td>
<td>1590</td>
<td>32</td>
<td>185</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>32</td>
<td>508</td>
<td>661</td>
<td>508</td>
<td>660</td>
<td>507</td>
<td>662</td>
<td>32</td>
<td>511</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>32</td>
<td>183</td>
<td>1630</td>
<td>184</td>
<td>1620</td>
<td>185</td>
<td>1610</td>
<td>32</td>
<td>146</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>32</td>
<td>551</td>
<td>703</td>
<td>550</td>
<td>704</td>
<td>550</td>
<td>704</td>
<td>32</td>
<td>529</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>32</td>
<td>61.4</td>
<td>10800</td>
<td>61.7</td>
<td>10700</td>
<td>61.7</td>
<td>10700</td>
<td>32</td>
<td>61.4</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>32</td>
<td>581</td>
<td>1220</td>
<td>580</td>
<td>1220</td>
<td>556</td>
<td>1270</td>
<td>32</td>
<td>554</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>32</td>
<td>401</td>
<td>499</td>
<td>400</td>
<td>500</td>
<td>401</td>
<td>499</td>
<td>32</td>
<td>364</td>
</tr>
<tr>
<td>473.astar</td>
<td>32</td>
<td>366</td>
<td>614</td>
<td>366</td>
<td>613</td>
<td>363</td>
<td>618</td>
<td>32</td>
<td>366</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>32</td>
<td>159</td>
<td>1390</td>
<td>159</td>
<td>1390</td>
<td>159</td>
<td>1390</td>
<td>32</td>
<td>159</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-j64x Tue Sep 12 23:14:37 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6134M CPU @ 3.20GHz
Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPECint_rate2006 = 1120
SPECint_rate_base2006 = 1060

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

2 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 8
siblings : 16
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27
cache size : 25344 KB

From /proc/meminfo
MemTotal: 394864336 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release*/etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or
  release.
  # Please check /etc/os-release for details about this release.

os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-j64x 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 12 23:12

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb7 xfs 416G 19G 398G 5% /home

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPECint_rate2006 = 1120
SPECint_rate_base2006 = 1060

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH =="/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
    echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
    shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
    numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
    icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
C++ benchmarks:
    icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPECint_rate2006 = 1120
SPECint_rate_base2006 = 1060

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Sep-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
- qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
- qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64

Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

SPECint_rate2006 = 1120
SPECint_rate_base2006 = 1060

CPU2006 license: 9019
Test date: Sep-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Peak Portability Flags (Continued)
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3
401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3
403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3
429.mcf: basepeak = yes
445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-mem-layout-trans=3
456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-qopt-mem-layout-trans=3
458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto-ilp32
-qopt-mem-layout-trans=3
462.libquantum: basepeak = yes
464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:
471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2)
-qopt-ra-region-strategy=block
-qopt-mem-layout-trans=3 -Wl,-z,muldefs
-L/sh10.2 -lsmartheap

Continued on next page
# SPEC CINT2006 Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6134M, 3.20GHz)

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>1120</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>1060</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

### Peak Optimization Flags (Continued)

- 473.astar: basepeak = yes
- 483.xalancbmk: basepeak = yes

### Peak Other Flags

- `C benchmarks:`
  - `403.gcc: -Dalloca=_alloca`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.  
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.  
Originally published on 12 October 2017.