Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6138, 2.00GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPECint\_rate2006 = 1900
SPECint\_rate_base2006 = 1800

Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Gold 6138</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Characteristics:</td>
<td>Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>CPU MHZ:</td>
<td>2000</td>
</tr>
<tr>
<td>FPU:</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled:</td>
<td>40 cores, 2 chips, 20 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable:</td>
<td>1,2 chips</td>
</tr>
<tr>
<td>Primary Cache:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache:</td>
<td>27.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other Cache:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Disk Subsystem:</td>
<td>1 x 480 GB SAS SSD</td>
</tr>
<tr>
<td>Other Hardware:</td>
<td>None</td>
</tr>
</tbody>
</table>

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2
## SPEC CINT2006 Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 6138, 2.00GHz)

<table>
<thead>
<tr>
<th>CPU2006 license:</th>
<th>9019</th>
</tr>
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<tbody>
<tr>
<td>Test sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPECint_rate2006 =** 1900  
**SPECint_rate_base2006 =** 1800

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>80</td>
<td>582</td>
<td>1340</td>
<td>584</td>
<td>1340</td>
<td>583</td>
<td>1340</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>401.bzip2</td>
<td>80</td>
<td><strong>950</strong></td>
<td><strong>813</strong></td>
<td>952</td>
<td>811</td>
<td>949</td>
<td>813</td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>403.gcc</td>
<td>80</td>
<td><strong>486</strong></td>
<td><strong>1330</strong></td>
<td>486</td>
<td>1330</td>
<td>484</td>
<td>1330</td>
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</tr>
<tr>
<td>429.mcf</td>
<td>80</td>
<td>289</td>
<td>2530</td>
<td>288</td>
<td><strong>2530</strong></td>
<td>288</td>
<td>2530</td>
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<td></td>
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<td></td>
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</tr>
<tr>
<td>445.gobmk</td>
<td>80</td>
<td>808</td>
<td>1040</td>
<td>808</td>
<td>1040</td>
<td>808</td>
<td>1040</td>
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<td></td>
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</tr>
<tr>
<td>456.hmmer</td>
<td>80</td>
<td>298</td>
<td>2500</td>
<td>297</td>
<td><strong>2510</strong></td>
<td>297</td>
<td>2520</td>
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<tr>
<td>458.sjeng</td>
<td>80</td>
<td>872</td>
<td>1110</td>
<td>871</td>
<td>1110</td>
<td>872</td>
<td><strong>1110</strong></td>
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<tr>
<td>462.libquantum</td>
<td>80</td>
<td>57.8</td>
<td>28700</td>
<td>57.6</td>
<td><strong>28800</strong></td>
<td>57.6</td>
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</tr>
<tr>
<td>464.h264ref</td>
<td>80</td>
<td>938</td>
<td>1890</td>
<td>943</td>
<td>1880</td>
<td><strong>941</strong></td>
<td><strong>1880</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>80</td>
<td><strong>508</strong></td>
<td><strong>984</strong></td>
<td>508</td>
<td>983</td>
<td>506</td>
<td>988</td>
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<td></td>
</tr>
<tr>
<td>473.astar</td>
<td>80</td>
<td>551</td>
<td>1020</td>
<td><strong>551</strong></td>
<td><strong>1020</strong></td>
<td>550</td>
<td>1020</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>80</td>
<td>272</td>
<td>2030</td>
<td><strong>271</strong></td>
<td><strong>2030</strong></td>
<td>271</td>
<td>2040</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

**BIOS Settings:**  
Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program `/home/cpu2006-1.2/config/sysinfo.rev6993`  
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)  
running on linux-79ix Mon Jul 31 23:02:37 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:  
http://www.spec.org/cpu2006/Docs/config/html#sysinfo

From `/proc/cpuinfo`  
model name : Intel(R) Xeon(R) Gold 6138 CPU @ 2.00GHz

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Cisco Systems
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Platform Notes (Continued)

  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
cache size : 28160 KB

From /proc/meminfo
MemTotal:       394653136 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

Additional information from dmidecode:
Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
  24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz
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Cisco Systems
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CPU2006 license: 9019
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Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "~/home/cpu2006-1.2/lib/ia32:~/home/cpu2006-1.2/lib/intel64:~/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runcspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3

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SPEC CINT2006 Result

Cisco Systems
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Software Availability: Apr-2017

Base Optimization Flags (Continued)

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: _Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
  400.perlbench: icc -m64
  401.bzip2: icc -m64
  456.hmmer: icc -m64
  458.sjeng: icc -m64

C++ benchmarks:
  icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
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Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
           -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
           -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
           -qopt-mem-layout-trans=3

403.gcc: -xCORE-AVX512 -ipo -O3 -no-prec-div
         -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
           -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
           -no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: -xCORE-AVX512 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
           -qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
           -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
           -no-prec-div(pass 2) -unroll4 -auto-ilp32
           -qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
             -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
             -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2)
             -qopt-ra-region-strategy=block
             -qopt-mem-layout-trans=3 -Wl,-z,muldefs
             -L/sh10.2 -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes
# SPEC CINT2006 Result

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6138, 2.00GHz)

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**Test date:** Aug-2017  
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**Software Availability:** Apr-2017

### Peak Other Flags

C benchmarks:

403.gcc -Dalloca=_alloca

---

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links: