Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Copyright 2006-2017 Standard Performance Evaluation Corporation

Test date: Jul-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

CPU Name: Intel Xeon Platinum 8168
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 2700
FPU: Integrated
CPU(s) enabled: 48 cores, 2 chips, 24 cores/chip, 2 threads/core
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: 33 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 600 GB SAS 10K RPM
Other Hardware: None

Operating System: SUSE Linux Enterprise Server 12 SP2 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2

SPECint®_rate2006 = 2610
SPECint_rate_base2006 = 2500
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

SPEC_int_rate2006 = 2610
SPECint_rate_base2006 = 2500

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Jul-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>96</td>
<td>464</td>
<td></td>
<td>463</td>
<td>1.00</td>
<td>463</td>
<td>1.00</td>
<td>96</td>
<td>381</td>
<td>1.00</td>
<td>2460</td>
<td>1.00</td>
<td>2460</td>
<td>1.00</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>96</td>
<td>814</td>
<td></td>
<td>813</td>
<td>1.00</td>
<td>812</td>
<td>1.00</td>
<td>96</td>
<td>779</td>
<td>1.00</td>
<td>777</td>
<td>1.00</td>
<td>1190</td>
<td>1.00</td>
</tr>
<tr>
<td>403.gcc</td>
<td>96</td>
<td>442</td>
<td></td>
<td>279</td>
<td>0.63</td>
<td>280</td>
<td>0.63</td>
<td>96</td>
<td>278</td>
<td>0.63</td>
<td>280</td>
<td>0.63</td>
<td>3130</td>
<td>1.00</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>96</td>
<td>627</td>
<td></td>
<td>627</td>
<td>1.00</td>
<td>627</td>
<td>1.00</td>
<td>96</td>
<td>629</td>
<td>1.00</td>
<td>629</td>
<td>1.00</td>
<td>1600</td>
<td>1.00</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>96</td>
<td>254</td>
<td></td>
<td>254</td>
<td>1.00</td>
<td>254</td>
<td>1.00</td>
<td>96</td>
<td>223</td>
<td>0.88</td>
<td>223</td>
<td>0.88</td>
<td>4020</td>
<td>1.00</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>96</td>
<td>677</td>
<td></td>
<td>677</td>
<td>1.00</td>
<td>677</td>
<td>1.00</td>
<td>96</td>
<td>629</td>
<td>0.93</td>
<td>629</td>
<td>0.93</td>
<td>1850</td>
<td>1.00</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>96</td>
<td>47.2</td>
<td></td>
<td>47.2</td>
<td>1.00</td>
<td>47.2</td>
<td>1.00</td>
<td>96</td>
<td>47.2</td>
<td>1.00</td>
<td>47.2</td>
<td>1.00</td>
<td>42100</td>
<td>1.00</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>96</td>
<td>732</td>
<td></td>
<td>735</td>
<td>1.00</td>
<td>737</td>
<td>1.00</td>
<td>96</td>
<td>706</td>
<td>0.95</td>
<td>710</td>
<td>1.00</td>
<td>2990</td>
<td>1.00</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>96</td>
<td>529</td>
<td></td>
<td>529</td>
<td>1.00</td>
<td>529</td>
<td>1.00</td>
<td>96</td>
<td>511</td>
<td>0.96</td>
<td>510</td>
<td>0.96</td>
<td>1180</td>
<td>1.00</td>
</tr>
<tr>
<td>473.astar</td>
<td>96</td>
<td>505</td>
<td></td>
<td>505</td>
<td>1.00</td>
<td>504</td>
<td>0.99</td>
<td>96</td>
<td>505</td>
<td>1.00</td>
<td>504</td>
<td>0.99</td>
<td>1330</td>
<td>1.00</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>96</td>
<td>255</td>
<td></td>
<td>255</td>
<td>1.00</td>
<td>254</td>
<td>0.99</td>
<td>96</td>
<td>255</td>
<td>1.00</td>
<td>254</td>
<td>0.99</td>
<td>2590</td>
<td>1.00</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
runtime on linux-omrt Wed Jul 19 01:08:20 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8168 CPU @ 2.70GHz
Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

SPECint_rate2006 = 2610
SPECint_rate_base2006 = 2500

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

2 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
cache size : 33792 KB

From /proc/meminfo
MemTotal: 394863572 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

uname -a:
9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jul 19 00:58

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 182G 19G 163G 11% /home

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to
Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

SPECint_rate2006 = 2610
SPECint_rate_base2006 = 2500

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "~/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
  icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

C++ benchmarks:
  icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

SPECint\_rate2006 = 2610
SPECint\_rate\_base2006 = 2500

CPU2006 license: 9019
Test date: Jul-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Peak Portability Flags

400.perlbench: -DSPEC\_CPU\_LP64 -DSPEC\_CPU\_LINUX\_X64
401.bzip2: -DSPEC\_CPU\_LP64
403.gcc: -D\_FILE\_OFFSET\_BITS=64
429.mcf: -D\_FILE\_OFFSET\_BITS=64
445.gobmk: -D\_FILE\_OFFSET\_BITS=64
456.hmmer: -DSPEC\_CPU\_LP64
458.sjeng: -DSPEC\_CPU\_LP64
462.libquantum: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX
464.h264ref: -D\_FILE\_OFFSET\_BITS=64
471.omnetpp: -D\_FILE\_OFFSET\_BITS=64
473.astar: -D\_FILE\_OFFSET\_BITS=64

Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

SPECint_rate2006 = 2610
SPECint_rate_base2006 = 2500

CPU2006 license: 9019
Test date: Jul-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Peak Portability Flags (Continued)
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
                -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
                -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3
401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
               -qopt-mem-layout-trans=3
403.gcc: -xCORE-AVX512 -ipo -O3 -no-prec-div
               -qopt-mem-layout-trans=3
429.mcf: basepeak = yes
445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -qopt-mem-layout-trans=3
456.hmmer: -xCORE-AVX512 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
               -qopt-mem-layout-trans=3
458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -unroll4 -auto-ilp32
               -qopt-mem-layout-trans=3
462.libquantum: basepeak = yes
464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:
471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512(pass 2)
              -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
              -no-prec-div(pass 2)
              -qopt-ra-region-strategy=block
              -qopt-mem-layout-trans=3 -Wl,-z,muldefs
              -L/sh10.2 -lsmartheap

Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8168, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>2610</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>2500</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jul-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags (Continued)

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 8 August 2017.