Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8180, 2.50GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: Jun-2017
Hardware Availability: Aug-2017

SPEClnt®_rate2006 = Not Run
SPEClnt_rate_base2006 = 2760

CPU Name: Intel Xeon Platinum 8180
CPU Characteristics: Intel Turbo Boost Technology up to 3.80 GHz
CPU MHz: 2500
FPU: Integrated
CPU(s) enabled: 56 cores, 2 chips, 28 cores/chip, 2 threads/core
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: 38.5 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 800 GB SSD SAS
Other Hardware: None

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64)
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran
Auto Parallel: No
File System: bfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2

Software

Hardware
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SPECint_rate2006 = Not Run
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Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
runtime on linux-nsv2 Mon Jun 26 11:36:37 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz
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Platform Notes (Continued)

2 "physical id"s (chips)
112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24
25 26 27 28 29 30

From /proc/meminfo

- MemTotal: 394864980 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
Continued on next page
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CPU2006 license: 9019  Test date: Jun-2017
Test sponsor: Cisco Systems  Hardware Availability: Aug-2017
Tested by: Cisco Systems  Software Availability: Sep-2017

Platform Notes (Continued)

hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1a.0.0607170937 06/07/2017
Memory:
  24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/intel/compilers_and_libraries_2018.0.082/linux/compiler/lib/ia32:/opt/intel/compilers_and_libraries_2018.0.082/linux/compiler/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2018.0.082/linux/lib/ia32

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2018.0.082/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
  401.bzip2: -D_FILE_OFFSET_BITS=64
  403.gcc: -D_FILE_OFFSET_BITS=64
  429.mcf: -D_FILE_OFFSET_BITS=64
  445.gobmk: -D_FILE_OFFSET_BITS=64
  456.hmmer: -D_FILE_OFFSET_BITS=64
  458.sjeng: -D_FILE_OFFSET_BITS=64
  462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
  464.h264ref: -D_FILE_OFFSET_BITS=64
  471.omnetpp: -D_FILE_OFFSET_BITS=64
  473.astar: -D_FILE_OFFSET_BITS=64
  483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
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Base Optimization Flags

C benchmarks:
- -xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3

C++ benchmarks:
- -xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
- -Wl,-z,muldefs -L/home/cpu2006-1.2/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
- 403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revG.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revG.xml

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For other inquiries, please contact webmaster@spec.org.

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