Huawei RH2288 V3(Intel Xeon E5-2630 v4)

SPECint\_rate2006 = \( \text{NC} \)

SPEC\_int\_rate\_base2006 = \( \text{NC} \)

**CPU2006 license:** 3175

**Test sponsor:** Huawei

**Tested by:** Huawei

**Test date:** Feb-2016

**Hardware Availability:** Mar-2016

**Software Availability:** Mar-2016

**Operating System:** Red Hat Enterprise Linux Server release 7.0 (Maipo) 3.10.0-123.el7.x86_64

**Compiler:** C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux

**Auto Parallel:** No

**File System:** xfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 32/64-bit

**Peak Pointers:** 32/64-bit

**Other Software:** Microquill SmartHeap V10.2

---

**Non-Compliant**

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by SPEC CPU rule 1.3.2 and the SPEC Open Systems Group policy on general availability.

---

**Hardware**

<table>
<thead>
<tr>
<th>Copies</th>
<th>Operating System</th>
<th>Compiler</th>
<th>Auto Parallel</th>
<th>File System</th>
<th>System State</th>
<th>Base Pointers</th>
<th>Peak Pointers</th>
<th>Other Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>Red Hat Enterprise Linux Server release 7.0 (Maipo) 3.10.0-123.el7.x86_64</td>
<td>C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux</td>
<td>No</td>
<td>xfs</td>
<td>Run level 3 (multi-user)</td>
<td>32/64-bit</td>
<td>32/64-bit</td>
<td>Microquill SmartHeap V10.2</td>
</tr>
</tbody>
</table>

**Software**

<table>
<thead>
<tr>
<th>CPU Name</th>
<th>CPU Characteristics</th>
<th>CPU MHz</th>
<th>FPU</th>
<th>CPU(s) enabled</th>
<th>CPU(s) orderable</th>
<th>Primary Cache</th>
<th>Secondary Cache</th>
<th>L3 Cache</th>
<th>Other Cache</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Xeon E5-2630 v4</td>
<td>Intel Turbo Boost Technology up to 3.10 GHz</td>
<td>2200</td>
<td>Integrated</td>
<td>20 cores, 2 chips, 10 cores/chip, 2 threads/core</td>
<td>1,2 chip</td>
<td>32 KB I + 32 KB D on chip per core</td>
<td>256 KB I+D on chip per core</td>
<td>25 MB I+D on chip per chip</td>
<td>None</td>
<td>256 GB (16 x 16 GB 2Rx4 PC4-2400T-R, running at 2133 MHz)</td>
</tr>
</tbody>
</table>

**Disk Subsystem:** 1 x 500 GB SATA, 7200 RPM

Continued on next page
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by SPEC CPU rule 1.3.2 and the SPEC Open Systems Group policy on general availability.

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The config file option 'submit' was used.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

- BIOS configuration:
  - Set Power Efficiency Mode to Performance
  - Set Snoop Mode to ES mode
  - Set Patrol Scrub to Disable

Sysinfo program /spec16/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on localhost.localdomain Wed Feb 17 06:28:17 2016

This section contains SUT (System Under Test) info as seen by

Continued on next page
Huawei
Huawei RH2288 V3(Intel Xeon E5-2630 v4)

**SPEC CINT2006 Result**

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>NC</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>NC</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 3175  
**Test sponsor:** Huawei  
**Tested by:** Huawei  
**Test date:** Feb-2016  
**Hardware Availability:** Mar-2016  
**Software Availability:** Mar-2016

**SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by [SPEC CPU rule 1.3.2](http://spec.org/cpu2006/Docs/runrules.html#rule_1.3.2) and the SPEC Open Systems Group policy on [general availability](https://www.spec.org/osg/policy.html#AppendixC).**

---

**Platform Notes (Continued)**

some common utilities. To remove or add to this section, see:  

From `/proc/cpuinfo`

- model name: Intel(R) Xeon(R) CPU E5-2630 v4 @ 2.20GHz
- 2 "physical id”s (chips)
- 40 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from `/proc/cpuinfo` might not be reliable. Use with caution.)
  - cpu cores: 10
  - siblings: 20
  - physical 0: cores 0 2 3 4 8 9 10 11 12
  - physical 1: cores 0 2 3 4 8 9 0 11 12
- cache size: 25600 KB

From `/proc/meminfo`

- MemTotal: 263568392 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release` /`etc/*version`

- os-release:
  - NAME="Red Hat Enterprise Linux Server"
  - VERSION="7.0 (Maipo)"
  - ID="rhel"
  - ID_LIKE="fedora"
  - VERSION_ID="7.0"
  - PRETTY_NAME="Red Hat Enterprise Linux Server 7.0 (Maipo)"
  - ANSI_COLOR="0;31"
  - CPE_NAME="cpe:/o:redhat:enterprise_linux:7.0:ga:server"

- run-level 3 Feb 17 06:23

- SPEC is set to: /spec16
  - Filesystem Type Size Used Avail Use% Mounted on
  - /dev/sda3 xfs 443G 9.7G 433G 3% /

Continued on next page
Huawei RH2288 V3(Intel Xeon E5-2630 v4)

SPECint_rate2006 = NC
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CPU2006 license: 3175
Test sponsor: Huawei
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Platform Notes (Continued)

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Insyde Corp. 7.11 02/14/2016
Memory:
8x Samsung M393A2G40EB1-CRC 16 GB 1 rank 2400 MHz, configured at 2133 MHz
8x Samsung M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz, configured at 2133 MHz

(End of data from sysinfo program)

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/spec16/libs/32:/spec16/libs/64:/spec16/sh"

Binaries compiled on system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numaclt i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
Huawei

Huawei RH2288 V3 (Intel Xeon E5-2630 v4)

CPU2006 license: 3175
Test sponsor: Huawei
Tested by: Huawei

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**Base Portability Flags**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX=IA32</td>
</tr>
<tr>
<td>401.bzip2:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>403.gcc:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>429.mcf:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>456.hmmer:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>458.sjeng:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>462.libquantum:</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX</td>
</tr>
<tr>
<td>464.h264ref:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>471.omnetpp:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>473.astar:</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>483.xalancbmk:</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX</td>
</tr>
</tbody>
</table>

**Base Optimization Flags**

C benchmarks:
- `xCORE-AVX2` -ipo -O3 -no-prec-div -opt-prefetch
- `opt-mem-layout-trans=3` -Wl,-z,muldefs -L/sh -lsmartheap

C++ benchmarks:
- `xCORE-AVX2` -ipo -O3 -no-prec-div -opt-prefetch
- `opt-mem-layout-trans=3` -W1,-z,muldefs -L/sh -lsmartheap

**Base Other Flags**

C benchmarks:
- `size: Dalloca=_alloca`

**Peak Compiler Invocation**

C benchmarks (except as noted below):

```
icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

400.perlbench: `icc -m64`

Continued on next page
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by SPEC CPU rule 1.3.2 and the SPEC Open Systems Group policy on general availability.

Peak Compiler Invocation (Continued)

```plaintext
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64
C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

Peak Portability Flags

```plaintext
400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
401.bzip2: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
456.hmmer: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
458.sjeng: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

Peak Optimization Flags

```plaintext
C benchmarks:
400.perlbench: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -auto-ilp32

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
-ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
-par-num-threads=1(pass 1) -prof-use(pass 2) -opt-prefetch
-auto-ilp32 -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div
```

Non-Compliant
## SPEC CINT2006 Result

### Huawei

**Huawei RH2288 V3 (Intel Xeon E5-2630 v4)**

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**CPU2006 license:** 3175  
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### Peak Optimization Flags (Continued)

- **429.mcf:** basepeak = yes
- **445.gobmk:** -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
  -prof-use(pass 2) -par-num-threads=1(pass 1) -ansi-alias
  -opt-mem-layout-trans=3
- **456.hmmer:** -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32
- **458.sjeng:** -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2) -unroll14
  -auto-ilp32
- **462.libquantum:** basepeak = yes
- **464.h264ref:** -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2) -unroll12
  -ansi-alias

### C++ benchmarks:

- **471.omnetpp:** -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2) -ansi-alias
  -opt-mem-region-strategy=block -Wl,-z,muldefs -L/sh -lsmartheap
- **479.astar:** basepeak = yes
- **493.xalancbmk:** basepeak = yes

### Peak Other Flags

- **C benchmarks:**
  - **403.gcc:** -Dalloca=_alloca
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by <a href="http://spec.org/cpu2006/Docs/runrules.html#rule_1.3.2">SPEC CPU rule 1.3.2</a> and the SPEC Open Systems Group policy on <a href="https://www.spec.org/osg/policy.html#AppendixC">general availability</a>.

The flags files that were used to format this result can be browsed at:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Huawei-Platform-Settings-BDW-V1.0.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Huawei-Platform-Settings-BDW-V1.0.xml