Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2640 v3 @ 2.60GHz)

SPECint\textsubscript{rate}2006 = 729
SPECint\textsubscript{rate\_base}2006 = 705

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2014
Hardware Availability: Sep-2014

Software Availability: Nov-2013

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECint\textsubscript{rate}2006</th>
<th>SPECint\textsubscript{rate_base}2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>32</td>
<td>363</td>
<td>32</td>
</tr>
<tr>
<td>bzip2</td>
<td>32</td>
<td>360</td>
<td>344</td>
</tr>
<tr>
<td>gcc</td>
<td>32</td>
<td>536</td>
<td>536</td>
</tr>
<tr>
<td>mcf</td>
<td>32</td>
<td>966</td>
<td>477</td>
</tr>
<tr>
<td>gobmk</td>
<td>32</td>
<td>466</td>
<td>1030</td>
</tr>
<tr>
<td>hmmer</td>
<td>32</td>
<td>1010</td>
<td>510</td>
</tr>
<tr>
<td>sjeng</td>
<td>32</td>
<td>495</td>
<td>495</td>
</tr>
<tr>
<td>libquantum</td>
<td>32</td>
<td>7140</td>
<td>5850</td>
</tr>
<tr>
<td>h264ref</td>
<td>32</td>
<td>809</td>
<td>405</td>
</tr>
<tr>
<td>omnetpp</td>
<td>32</td>
<td>388</td>
<td>387</td>
</tr>
<tr>
<td>astar</td>
<td>32</td>
<td>780</td>
<td>780</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>32</td>
<td>780</td>
<td>780</td>
</tr>
</tbody>
</table>

Hardware:
- CPU Name: Intel Xeon E5-2640 v3
- CPU Characteristics: Intel Turbo Boost Technology up to 3.40 GHz
- CPU MHz: 2600
- FPU: Integrated
- CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip, 2 threads/core
- CPU(s) orderable: 1,2 chips
- Primary Cache: 32 KB I + 32 KB D on chip per core
- Secondary Cache: 256 KB I+D on chip per core
- L3 Cache: 20 MB I+D on chip per chip
- Other Cache: None
- Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2133P-R, running at 1866 MHz)
- Disk Subsystem: 1 x 300GB SAS, 15K RPM
- Other Hardware: None

Software:
- Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
- Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
- Auto Parallel: No
- File System: ext4
- System State: Run level 3 (multi-user)
- Base Pointers: 32-bit
- Peak Pointers: 32/64-bit
- Other Software: Microquill SmartHeap V10.0
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2640 v3 @ 2.60GHz)

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SPECint_rate_base2006 = 705

CPU2006 license: 9019
Test sponsor: Cisco Systems
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<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>32</td>
<td>587</td>
<td>533</td>
<td>586</td>
<td>533</td>
<td>588</td>
<td>532</td>
<td>589</td>
<td>533</td>
<td>588</td>
<td>532</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>32</td>
<td>897</td>
<td>344</td>
<td>897</td>
<td>344</td>
<td>897</td>
<td>344</td>
<td>897</td>
<td>344</td>
<td>897</td>
<td>344</td>
</tr>
<tr>
<td>403.gcc</td>
<td>32</td>
<td>480</td>
<td>537</td>
<td>481</td>
<td>536</td>
<td>485</td>
<td>531</td>
<td>484</td>
<td>533</td>
<td>481</td>
<td>536</td>
</tr>
<tr>
<td>429.mcf</td>
<td>32</td>
<td>302</td>
<td>966</td>
<td>302</td>
<td>966</td>
<td>304</td>
<td>961</td>
<td>302</td>
<td>966</td>
<td>302</td>
<td>966</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>32</td>
<td>720</td>
<td>467</td>
<td>720</td>
<td>466</td>
<td>720</td>
<td>466</td>
<td>720</td>
<td>466</td>
<td>720</td>
<td>466</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>32</td>
<td>294</td>
<td>1020</td>
<td>298</td>
<td>1000</td>
<td>295</td>
<td>1010</td>
<td>288</td>
<td>1040</td>
<td>289</td>
<td>1030</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>32</td>
<td>783</td>
<td>495</td>
<td>782</td>
<td>495</td>
<td>782</td>
<td>495</td>
<td>774</td>
<td>519</td>
<td>759</td>
<td>510</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>32</td>
<td>93.3</td>
<td>7110</td>
<td>92.9</td>
<td>7140</td>
<td>92.7</td>
<td>7150</td>
<td>92.9</td>
<td>7140</td>
<td>92.7</td>
<td>7150</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>32</td>
<td>875</td>
<td>809</td>
<td>882</td>
<td>803</td>
<td>865</td>
<td>819</td>
<td>829</td>
<td>855</td>
<td>833</td>
<td>850</td>
</tr>
<tr>
<td>471.onetopp</td>
<td>32</td>
<td>520</td>
<td>385</td>
<td>515</td>
<td>388</td>
<td>516</td>
<td>388</td>
<td>492</td>
<td>406</td>
<td>494</td>
<td>405</td>
</tr>
<tr>
<td>473.astar</td>
<td>32</td>
<td>584</td>
<td>385</td>
<td>580</td>
<td>387</td>
<td>580</td>
<td>388</td>
<td>584</td>
<td>385</td>
<td>580</td>
<td>387</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>32</td>
<td>283</td>
<td>781</td>
<td>283</td>
<td>780</td>
<td>283</td>
<td>780</td>
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<td>780</td>
</tr>
</tbody>
</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
CPU performance set to HPC
Power Technology set to Custom
Processor Power State C6 set to Disabled
Energy Performance BIAS setting set to Performance
Memory RAS configuration set to Maximum Performance
Snoop Mode set to Early Snoop
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on rhe165 Sat Dec  6 11:21:14 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2640 v3 @ 2.60GHz
2 "physical id"s (chips)

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Platform Notes (Continued)

32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)

```
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
cache size : 20480 KB
```

From /proc/meminfo
MemTotal: 264258848 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```
/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)
```

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)

```
uname -a:
Linux rhel65 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013 x86_64
x86_64 x86_64 GNU/Linux
```
run-level 3 Dec 6 11:20

SPEC is set to: /opt/cpu2006-1.2
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 ext4 245G 19G 215G 8% /
```

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C240M4.2.0.3c.0.091920142008 09/19/2014
Memory:
16x 0xCE00 M393A2G40DB0-CPB 16 GB 1866 MHz 2 rank
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB
memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:

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Standard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2640 v3 @ 2.60GHz)

| SPECint_rate2006 | 729 |
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General Notes (Continued)

```
echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.: numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
- `icc  -m32`

C++ benchmarks:
- `icpc  -m32`

Base Portability Flags

- 400.perlbench: -DSPEC_CPU_LINUX_IA32
- 462.libquantum: -DSPEC_CPU_LINUX
- 483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
- `xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch`
- `opt-mem-layout-trans=3`

C++ benchmarks:
- `xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch`
- `opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap`

Base Other Flags

C benchmarks:
- `403.gcc: -Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
- `icc  -m32`
- `400.perlbench: icc  -m64`

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Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2640 v3 @ 2.60GHz)

<table>
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<th>729</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>705</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

**Peak Compiler Invocation (Continued)**

```plaintext
 401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64
```

C++ benchmarks:
```plaintext
icpc -m32
```

**Peak Portability Flags**

```plaintext
400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX
```

**Peak Optimization Flags**

C benchmarks:
```plaintext
400.perlbench: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32
401.bzip2: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias
403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div
429.mcf: basepeak = yes
445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -opt-mem-layout-trans=3
456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32
458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32
462.libquantum: basepeak = yes
```

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Peak Optimization Flags (Continued)

464.h264ref: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalanchbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.xml

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For other inquiries, please contact webmaster@spec.org.

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