



SPEC[®] CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint[®]_rate2006 = 901

SPECint_rate_base2006 = 869

CPU2006 license: 9019

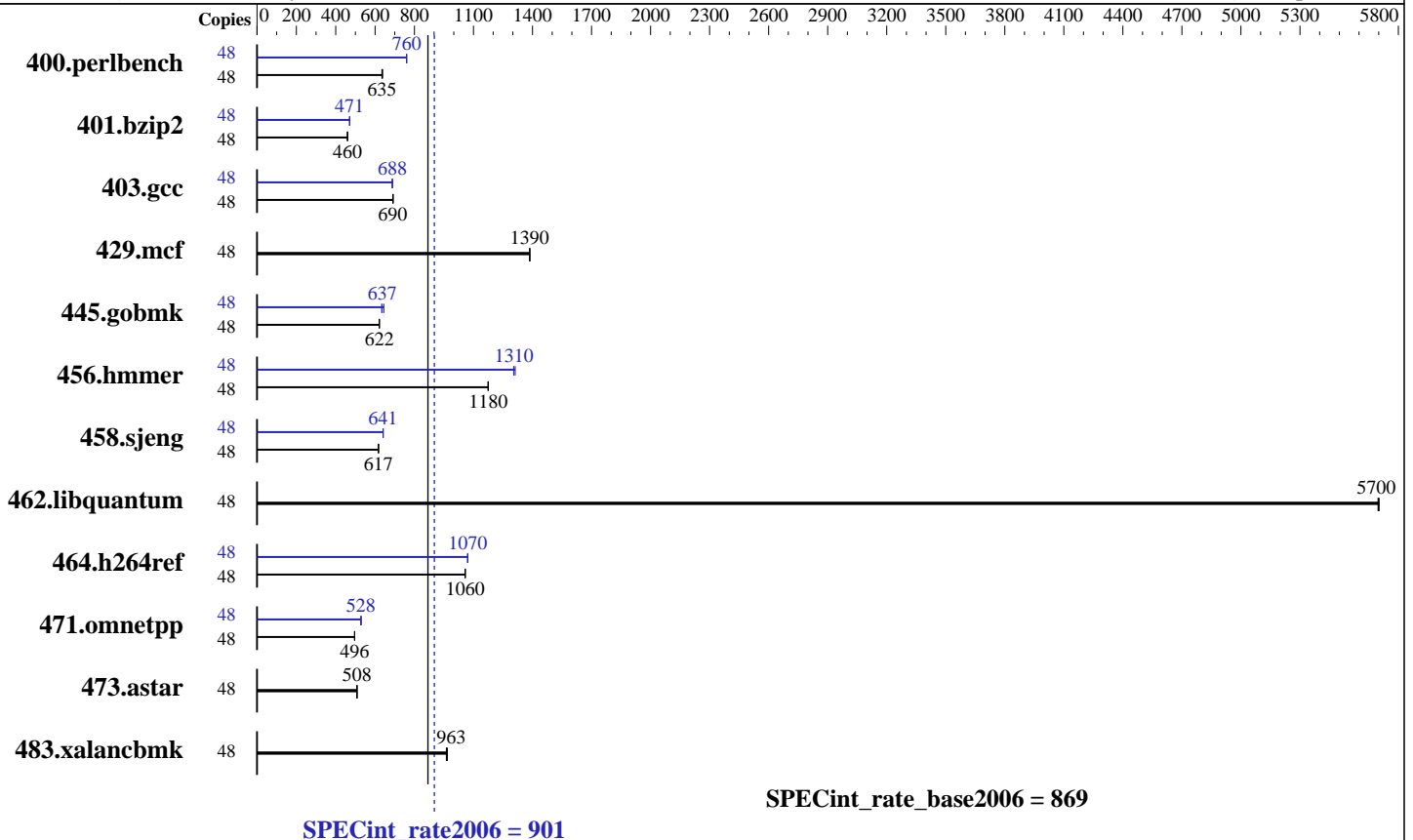
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: May-2014

Hardware Availability: Dec-2013

Software Availability: Apr-2014



Hardware

CPU Name: Intel Xeon E5-4607 v2
 CPU Characteristics:
 CPU MHz: 2600
 FPU: Integrated
 CPU(s) enabled: 24 cores, 4 chips, 6 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2,3,4 chip
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 15 MB I+D on chip per chip
 Other Cache: None
 Memory: 256 GB (32 x 8 GB 2Rx4 PC3-14900R-13, ECC, running at 1333 MHz and CL9)
 Disk Subsystem: 1 X 300 GB 15000 RPM SAS
 Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
 2.6.32-431.el6.x86_64
 Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
 Auto Parallel: No
 File System: ext4
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint_rate2006 = 901

SPECint_rate_base2006 = 869

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2014
Hardware Availability: Dec-2013
Software Availability: Apr-2014

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	48	738	635	739	635	734	639	48	617	760	617	760	617	760
401.bzip2	48	1005	461	1006	460	1010	459	48	983	471	985	470	984	471
403.gcc	48	558	693	560	690	560	690	48	561	688	563	687	561	688
429.mcf	48	316	1390	316	1390	316	1390	48	316	1390	316	1390	316	1390
445.gobmk	48	811	621	809	622	810	622	48	781	645	795	633	791	637
456.hammer	48	381	1180	382	1170	381	1180	48	343	1310	343	1300	341	1310
458.sjeng	48	940	618	942	617	941	617	48	906	641	906	641	906	641
462.libquantum	48	175	5700	174	5700	175	5700	48	175	5700	174	5700	175	5700
464.h264ref	48	1004	1060	1005	1060	1003	1060	48	993	1070	992	1070	991	1070
471.omnetpp	48	605	496	604	496	605	496	48	567	529	568	528	568	528
473.astar	48	664	508	662	509	664	508	48	664	508	662	509	664	508
483.xalancbmk	48	344	962	342	967	344	963	48	344	962	342	967	344	963

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disabled
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
Sysinfo program /opt/cpu2006-1.4/config/sysinfo.rev6818
\$Rev: 6818 \$ \$Date:: 2012-07-17 #\$ e86d102572650a6e4d596a3cee98f191
running on b420m3 Mon May 19 20:59:00 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4607 v2 @ 2.60GHz
Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint_rate2006 = 901

SPECint_rate_base2006 = 869

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2014
Hardware Availability: Dec-2013
Software Availability: Apr-2014

Platform Notes (Continued)

```

4 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 6
siblings  : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
physical 2: cores 0 1 2 3 4 5
physical 3: cores 0 1 2 3 4 5
cache size : 15360 KB

From /proc/meminfo
MemTotal:      264499732 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

uname -a:
Linux b420m3 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013 x86_64
x86_64 x86_64 GNU/Linux

run-level 3 May 19 20:52

SPEC is set to: /opt/cpu2006-1.4
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal       ext4  275G   82G  179G  32% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. B420M3.2.2.1.8.042120142113 04/21/2014
Memory:
32x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1333 MHz 2 rank
16x NO DIMM NO DIMM

(End of data from sysinfo program)

```

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.4/libs/32:/opt/cpu2006-1.4/libs/64:/opt/cpu2006-1.4/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint_rate2006 = 901

SPECint_rate_base2006 = 869

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: May-2014

Hardware Availability: Dec-2013

Software Availability: Apr-2014

General Notes (Continued)

Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint_rate2006 = 901

SPECint_rate_base2006 = 869

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: May-2014

Hardware Availability: Dec-2013

Software Availability: Apr-2014

Peak Compiler Invocation (Continued)

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

401.bzip2: -DSPEC_CPU_LP64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 901

Cisco UCS B420 M3 (Intel Xeon E5-4607 v2, 2.60 GHz)

SPECint_rate_base2006 = 869

CPU2006 license: 9019

Test date: May-2014

Test sponsor: Cisco Systems

Hardware Availability: Dec-2013

Tested by: Cisco Systems

Software Availability: Apr-2014

Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Fri Jul 25 00:14:06 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 1 July 2014.