Cisco UCS C22 M3 (Intel Xeon E5-2407, 2.20 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

CPU Name: Intel Xeon E5-2407
CPU Characteristics: Integrated
CPU(s) enabled: 4 cores, 1 chip, 4 cores/chip
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 10 MB I+D on chip per chip
Other Cache: None
Memory: 48 GB (6 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1067 MHz and CL7)
Disk Subsystem: 1 X 146 GB 15000 RPM SAS
Other Hardware: None

Hardware

Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)
Compiler: C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V9.01

Software

SPECint\_rate2006 = 106
SPECint\_rate_base2006 = 102
Cisco Systems

Cisco UCS C22 M3 (Intel Xeon E5-2407, 2.20 GHz)

SPEC CINT2006 Result

CPU2006 license: 9019
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SPECint_rate2006 = 106
SPECint_rate_base2006 = 102

Results Table

<table>
<thead>
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<th>Benchmark</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>445.gobmk</td>
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<td>64.5</td>
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<td>456.hmmer</td>
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<td>462.libquantum</td>
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<td>464.h264ref</td>
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<td>471.omnetpp</td>
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<tr>
<td>483.xalancbmk</td>
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<td>121</td>
<td>228</td>
<td>121</td>
<td>229</td>
<td>121</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdf5032aaa42e583f96b07f99d3
running on C22-M3 Tue Dec 11 19:43:15 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E5-2407 0 @ 2.20GHz
  1 "physical id"s (chips)
  4 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4

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CPU2006 license: 9019
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Platform Notes (Continued)

physical 0: cores 0 1 2 3
  cache size : 10240 KB

From /proc/meminfo
  MemTotal: 49403308 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
  Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
  redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
  system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

uname -a:
  Linux C22-M3 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13 EST 2011 x86_64
  x86_64 x86_64 GNU/Linux

run-level 3 Dec 11 19:41

SPEC is set to: /opt/cpu2006-1.2
  Filesystem    Type    Size  Used Avail Use% Mounted on
  /dev/sda1     ext4    134G  9.9G  118G   8% /

Additional information from dmidecode:
  Memory:
    6x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2
Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
  echo 1> /proc/sys/vm/drop_caches

Base Compiler Invocation

C benchmarks:
  icc  -m32

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Cisco Systems
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Test date: Dec-2012
Hardware Availability: Sep-2012
Software Availability: Feb-2012

Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32
400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64
C++ benchmarks:
icpc -m32
Cisco Systems
Cisco UCS C22 M3 (Intel Xeon E5-2407, 2.20 GHz)

**SPEC CINT2006 Result**

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**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test date:** Dec-2012  
**Hardware Availability:** Sep-2012  
**Software Availability:** Feb-2012

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### Peak Portability Flags

- **400.perlbench:** -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
- **401.bzip2:** -DSPEC_CPU_LP64
- **456.hmmer:** -DSPEC_CPU_LP64
- **458.sjeng:** -DSPEC_CPU_LP64
- **462.libquantum:** -DSPEC_CPU_LINUX
- **483.xalancbmk:** -DSPEC_CPU_LINUX

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### Peak Optimization Flags

#### C benchmarks:

- **400.perlbench:** -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32
- **401.bzip2:** -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias
- **403.gcc:** -xSSE4.2 -ipo -O3 -no-prec-div
- **429.mcf:** basepeak = yes
- **445.gobmk:** -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -opt-mem-layout-trans=3
- **456.hmmer:** -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
- **458.sjeng:** -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32
- **462.libquantum:** basepeak = yes
- **464.h264ref:** -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll2 -ansi-alias

#### C++ benchmarks:

- **471.omnetpp:** -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/smartheap -lsmartheap
- **473.astar:** basepeak = yes

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Cisco Systems

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Software Availability: Feb-2012

Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.xml

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Tested with SPEC CPU2006 v1.2.
Originally published on 2 January 2013.