Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)  

<table>
<thead>
<tr>
<th>SPECint®_rate2006</th>
<th>458</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>440</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019  
Test date: Dec-2012  
Tested by: Cisco Systems  
Software Availability: Feb-2012

| Software | CPU Name: Intel Xeon E5-4603  
CPU Characteristics:  
CPU(s) enabled: 16 cores, 4 chips, 4 cores/chip, 2 threads/core  
Primary Cache: 32 KB I + 32 KB D on chip per core  
Secondary Cache: 256 KB I+D on chip per core  
L3 Cache: 10 MB I+D on chip per chip  
Other Cache: None  
Memory: 256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1333 MHz and CL7)  
Disk Subsystem: 1 X 300 GB 15000 RPM SAS  
Other Hardware: None  
Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)  
Compiler: C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux  
Auto Parallel: No  
File System: ext4  
System State: Run level 3 (multi-user)  
Base Pointers: 32-bit  
Peak Pointers: 32/64-bit  
Other Software: Microquill SmartHeap V9.01 |

Hardware

![Graph showing SPECint results with benchmarks and their scores]
Cisco Systems
Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)

**SPEC CINT2006 Result**

**SPECint_rate2006** = 458
**SPECint_rate_base2006** = 440

**CPU2006 license:** 9019
**Test sponsor:** Cisco Systems
**Tested by:** Cisco Systems

**Test date:** Dec-2012
**Hardware Availability:** Sep-2012
**Software Availability:** Feb-2012

---

### Results Table

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<th>Seconds</th>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### Platform Notes

BIOS Configuration:
- Hyper-Threading set to Enabled
- Processor C6 Report set to Disabled
- Processor C1E set to Disabled
- CPU Performance set to HPC
- LV DDR Mode set to Performance-mode

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800

$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdFF5032aaa42e583f96b07f99d3
running on SPECCPU-M3 Sat Dec 1 23:41:19 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

    model name : Intel(R) Xeon(R) CPU E5-4603 0 @ 2.00GHz
        4 "physical id"s (chips)

Continued on next page
Cisco Systems

Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)

SPECint_rate2006 = 458
SPECint_rate_base2006 = 440

CPU2006 license: 9019
Test date: Dec-2012
Test sponsor: Cisco Systems
Hardware Availability: Sep-2012
Tested by: Cisco Systems
Software Availability: Feb-2012

Platform Notes (Continued)

32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 4
siblings : 8
physical 0: cores 0 1 2 3
physical 1: cores 0 1 2 3
physical 2: cores 0 1 2 3
physical 3: cores 0 1 2 3
cache size : 10240 KB

From /proc/meminfo
MemTotal: 264505740 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

uname -a:
Linux SPECCPU-M3 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13 EST 2011
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Nov 29 14:27

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 ext4 1.1T 7.7G 1.1T 1% /

Additional information from dmidecode:
Memory:
32x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank
(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL6.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
Cisco Systems
Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)  

---

**SPEC CINT2006 Result**

**SPECint_rate2006** = 458  
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---

**Base Compiler Invocation**

- C benchmarks: `icc -m32`
- C++ benchmarks: `icpc -m32`

---

**Base Portability Flags**

- 400.perlbench: `-DSPEC_CPU_LINUX_IA32`
- 462.libquantum: `-DSPEC_CPU_LINUX`
- 483.xalancbmk: `-DSPEC_CPU_LINUX`

---

**Base Optimization Flags**

**C benchmarks:**

- `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3`

**C++ benchmarks:**

- `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3`
- `-Wl,-z,muldefs -L/smartheap -lsmartheap`

---

**Base Other Flags**

- C benchmarks:
  - `403.gcc: -Dalloca=_alloca`

---

**Peak Compiler Invocation**

**C benchmarks (except as noted below):**

- `icc -m32`
  - 400.perlbench: `icc -m64`
  - 401.bzip2: `icc -m64`
  - 456.hmmer: `icc -m64`
  - 458.sjeng: `icc -m64`

**C++ benchmarks:**

- `icpc -m32`
Cisco Systems
Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)

**SPECint_rate2006 =** 458  
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CPU2006 license: 9019  
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Tested by: Cisco Systems

Test date: Dec-2012  
Hardware Availability: Sep-2012  
Software Availability: Feb-2012

---

**Peak Portability Flags**

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

---

**Peak Optimization Flags**

C benchmarks:

400.perlbench: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -no-prec-div (pass 2) -prof-use (pass 2) -auto-ilp32

401.bzip2: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -no-prec-div (pass 2) -prof-use (pass 2) -opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2 (pass 2) -prof-gen (pass 1) -prof-use (pass 2) -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -no-prec-div (pass 2) -prof-use (pass 2) -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -no-prec-div (pass 2) -prof-use (pass 2) -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -no-prec-div (pass 2) -prof-use (pass 2) -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/smartheap -lsmartheap

473.astar: basepeak = yes

Continued on next page
Cisco UCS B420 M3 (Intel Xeon E5-4603, 2.00 GHz)

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Software Availability: Feb-2012

Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml

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For questions about this result, please contact the tester. For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
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