



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

SPECint_rate2006 = 959

SPECint_rate_base2006 = 914

CPU2006 license: 9019

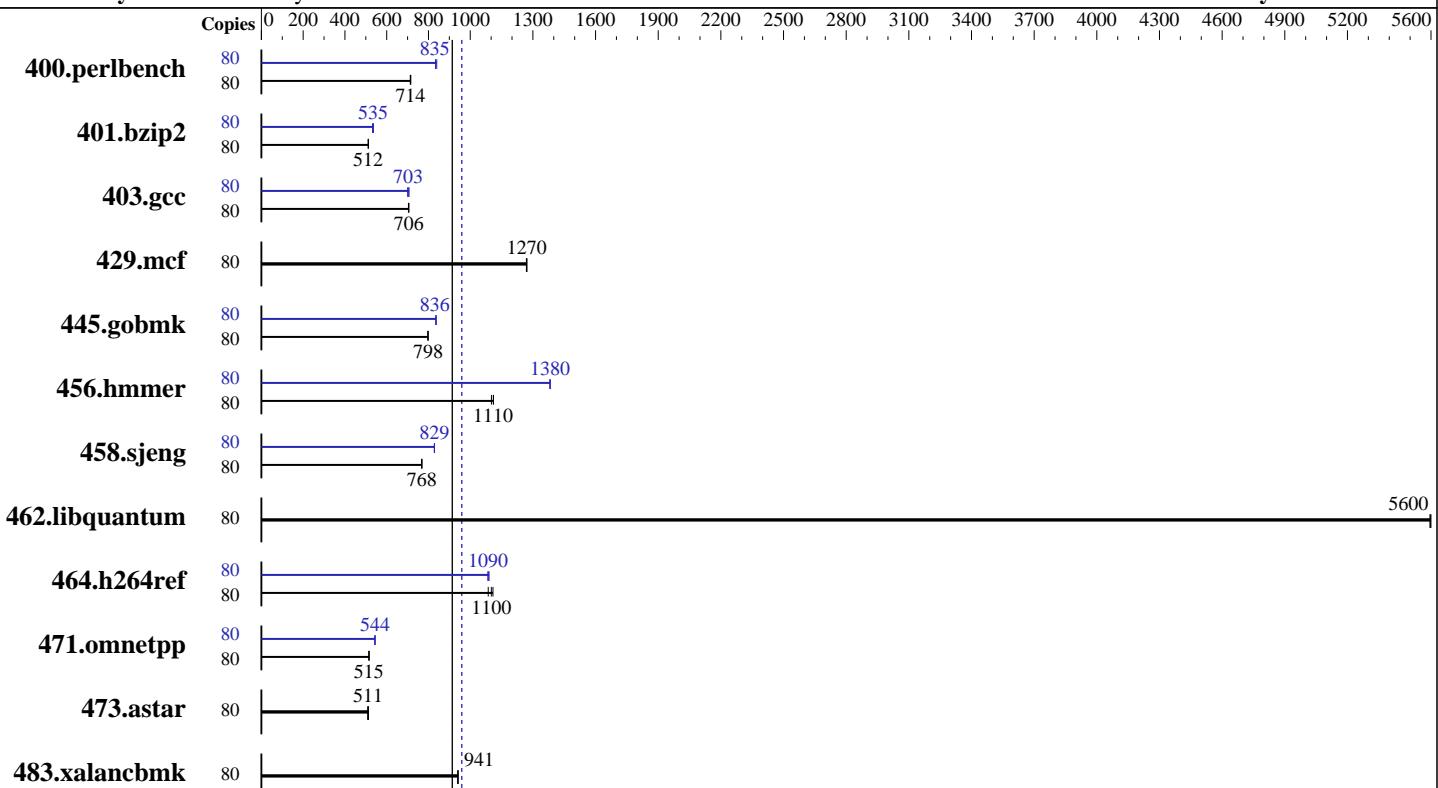
Test date: Jan-2012

Test sponsor: Cisco Systems

Hardware Availability: May-2011

Tested by: Cisco Systems

Software Availability: Oct-2011



SPECint_rate_base2006 = 914

SPECint_rate2006 = 959

Hardware

CPU Name: Intel Xeon E7-4850
CPU Characteristics: Intel Turbo Boost Technology up to 2.40 GHz
CPU MHz: 2000
FPU: Integrated
CPU(s) enabled: 40 cores, 4 chips, 10 cores/chip, 2 threads/core
CPU(s) orderable: 1,2,3,4 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 24 MB I+D on chip per chip
Other Cache: None
Memory: 512 GB (32 x 16 GB 4Rx4 PC3-8500R-9, ECC)
Disk Subsystem: 600 GB SAS 10K RPM
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.1 (Santiago)
Compiler: 2.6.32-131.0.15.el6.x86_64
C/C++: Version 12.1.0.225 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V9.01



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

SPECint_rate2006 = 959

SPECint_rate_base2006 = 914

CPU2006 license: 9019

Test date: Jan-2012

Test sponsor: Cisco Systems

Hardware Availability: May-2011

Tested by: Cisco Systems

Software Availability: Oct-2011

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	80	<u>1095</u>	<u>714</u>	1096	713	1092	715	80	<u>931</u>	<u>840</u>	<u>937</u>	<u>834</u>	<u>936</u>	<u>835</u>
401.bzip2	80	1508	512	<u>1508</u>	<u>512</u>	1507	512	80	<u>1442</u>	<u>535</u>	1440	536	1450	532
403.gcc	80	913	706	915	704	<u>913</u>	<u>706</u>	80	920	700	<u>916</u>	<u>703</u>	911	707
429.mcf	80	574	1270	575	1270	<u>574</u>	<u>1270</u>	80	574	1270	575	1270	<u>574</u>	<u>1270</u>
445.gobmk	80	1052	797	1051	798	<u>1052</u>	<u>798</u>	80	<u>1004</u>	<u>836</u>	1004	836	1003	836
456.hmmer	80	678	1100	<u>672</u>	<u>1110</u>	672	1110	80	<u>540</u>	<u>1380</u>	540	1380	540	1380
458.sjeng	80	1261	768	<u>1261</u>	<u>768</u>	1259	769	80	1169	828	1168	829	<u>1168</u>	<u>829</u>
462.libquantum	80	296	5600	<u>296</u>	<u>5600</u>	296	5600	80	296	5600	<u>296</u>	<u>5600</u>	296	5600
464.h264ref	80	1630	1090	<u>1608</u>	<u>1100</u>	1597	1110	80	<u>1630</u>	<u>1090</u>	1632	1080	1624	1090
471.omnetpp	80	971	515	<u>971</u>	<u>515</u>	969	516	80	<u>919</u>	<u>544</u>	919	544	921	543
473.astar	80	<u>1098</u>	<u>511</u>	1103	509	1096	513	80	<u>1098</u>	<u>511</u>	1103	509	1096	513
483.xalancbmk	80	<u>587</u>	<u>941</u>	587	941	586	942	80	<u>587</u>	<u>941</u>	587	941	586	942

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

```
Sysinfo program /opt/cpu2006/config/sysinfo.rev6800
$Rev: 6800 $ $Date::: 2011-10-11 #$
running on localhost.localdomain Tue Jan 10 18:43:49 2012
```

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7- 4850 @ 2.00GHz
        4 "physical id"s (chips)
        80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
        cpu cores : 10
        siblings  : 20
```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

SPECint_rate2006 = 959

CPU2006 license: 9019

Test date: Jan-2012

Test sponsor: Cisco Systems

Hardware Availability: May-2011

Tested by: Cisco Systems

Software Availability: Oct-2011

Platform Notes (Continued)

```
physical 0: cores 0 1 2 8 9 16 17 18 24 25
physical 1: cores 0 1 2 8 9 16 17 18 24 25
physical 2: cores 0 1 2 8 9 16 17 18 24 25
physical 3: cores 0 1 2 8 9 16 17 18 24 25
cache size : 24576 kB

From /proc/meminfo
MemTotal:      529231820 kB
HugePages_Total:      0
Hugepagesize:     2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.1 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.1 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.1 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

uname -a:
Linux localhost.localdomain 2.6.32-131.0.15.el6.x86_64 #1 SMP Tue May 10
15:42:40 EDT 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 10 18:19

SPEC is set to: /opt/cpu2006
Filesystem      Type    Size  Used Avail Use% Mounted on
/dev/sdal      ext4    134G   5.8G  122G   5%  /


Additional information from dmidecode:

(End of data from sysinfo program)
```

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006/libs/32:/opt/cpu2006/libs/64"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RHEL5.5

Transparent Huge Pages enabled with:

```
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
```

Filesystem page cache cleared with:

```
echo 1> /proc/sys/vm/drop_caches
```

runspec command invoked through numactl i.e.:

```
numactl --interleave=all runspec <etc>
```



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 959

SPECint_rate_base2006 = 914

Test date: Jan-2012

Hardware Availability: May-2011

Software Availability: Oct-2011

Base Compiler Invocation

C benchmarks:

icc -m32

C++ benchmarks:

icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 959

SPECint_rate_base2006 = 914

Test date: Jan-2012

Hardware Availability: May-2011

Software Availability: Oct-2011

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll14 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll12 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/smartheap -lsmartheap

473.astar: basepeak = yes

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

SPECint_rate2006 = 959

SPECint_rate_base2006 = 914

Test date: Jan-2012

Hardware Availability: May-2011

Software Availability: Oct-2011

Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=__alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Thu Jul 24 03:40:08 2014 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 15 February 2012.