SPEC® CINT2006 Result

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IBM Corporation

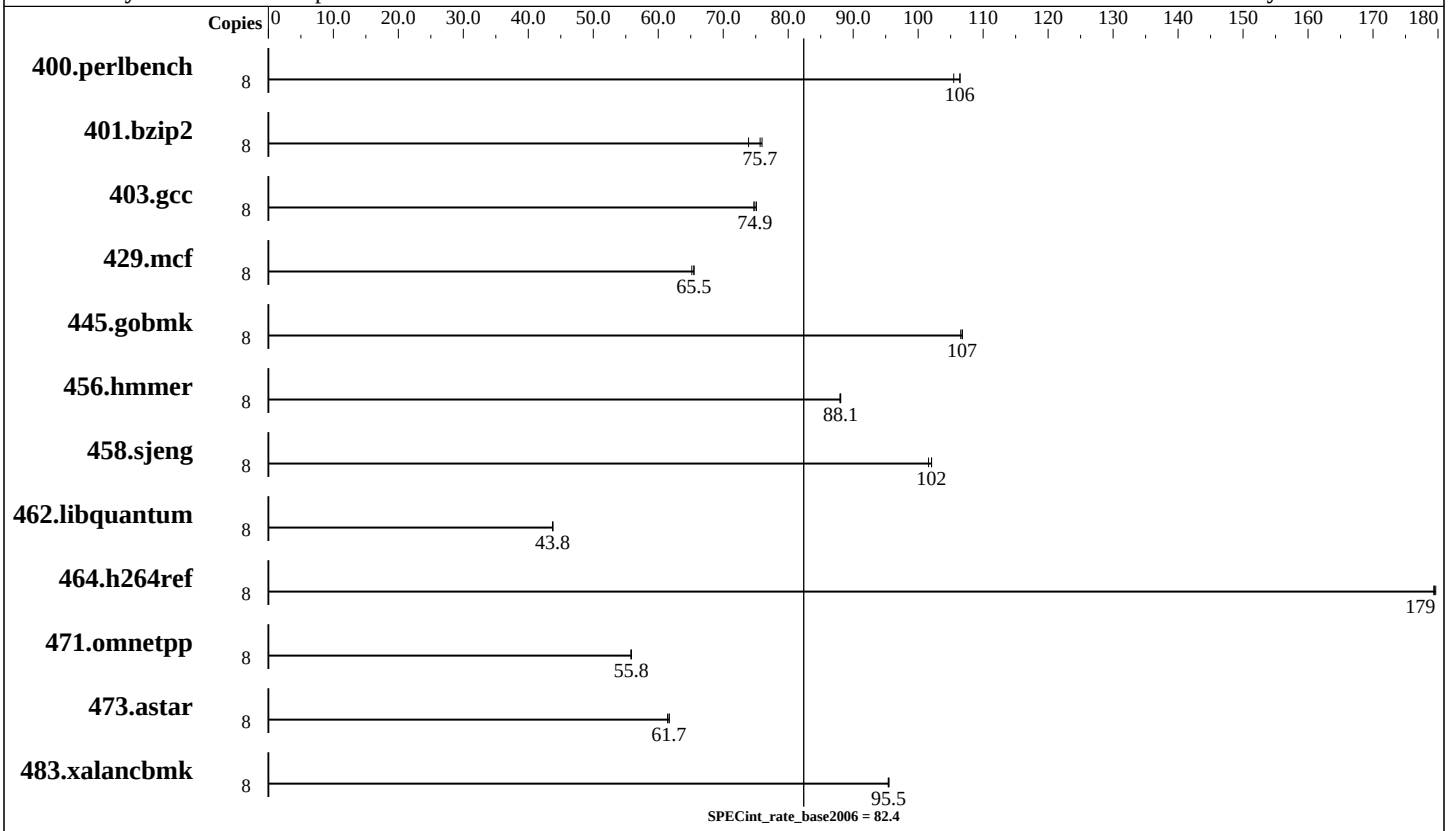
IBM BladeCenter HS21 XM (Intel Xeon L5408)

SPECint®_rate2006 = Not Run

SPECint_rate_base2006 = 82.4

CPU2006 license: 11
Test sponsor: IBM Corporation
Tested by: IBM Corporation

Test date: May-2008
Hardware Availability: Jul-2008
Software Availability: Nov-2007



Hardware

CPU Name:	Intel Xeon L5408
CPU Characteristics:	1066MHz system bus
CPU MHz:	2133
FPU:	Integrated
CPU(s) enabled:	8 cores, 2 chips, 4 cores/chip
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	12 MB I+D on chip per chip, 6 MB shared / 2 cores
L3 Cache:	None
Other Cache:	None
Memory:	16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem:	1 x 36 GB SAS, 10000 RPM
Other Hardware:	None

Software

Operating System:	SuSE Linux Enterprise Server 10 (x86_64), kernel 2.6.16.21-0.8-smp
Compiler:	Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel:	No
File System:	ReiserFS
System State:	Multi-user, run level 3
Base Pointers:	32-bit
Peak Pointers:	Not Applicable
Other Software:	MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	741	105	734	106	**734**	**106**							
401.bzip2	8	1016	76.0	1045	73.9	**1020**	**75.7**							
403.gcc	8	857	75.1	**860**	**74.9**	862	74.7							
429.mcf	8	**1114**	**65.5**	1120	65.2	1114	65.5							
445.gobmk	8	786	107	**786**	**107**	788	107							
456.hmmer	8	**848**	**88.1**	849	88.0	847	88.1							
458.sjeng	8	953	102	**949**	**102**	948	102							
462.libquantum	8	**3787**	**43.8**	3789	43.7	3787	43.8							
464.h264ref	8	**986**	**179**	987	179	985	180							
471.omnetpp	8	895	55.8	**895**	**55.8**	896	55.8							
473.astar	8	914	61.4	**911**	**61.7**	910	61.7							
483.xalancbmk	8	578	95.5	**578**	**95.5**	579	95.4							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
All benchmarks compiled in 32-bit mode
Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
taskset utility used to bind CPU(s) to processes
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:
`-fast -inline-calloc -opt-malloc-options=3`

Continued on next page

Base Optimization Flags (Continued)

C++ benchmarks:
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
-L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10.1-int-linux64-revC.20090713.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10.1-int-linux64-revC.20090713.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.0.
Report generated on Tue Jul 22 17:48:42 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 25 June 2008.