SPEC® CINT2006 Result

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IBM Corporation

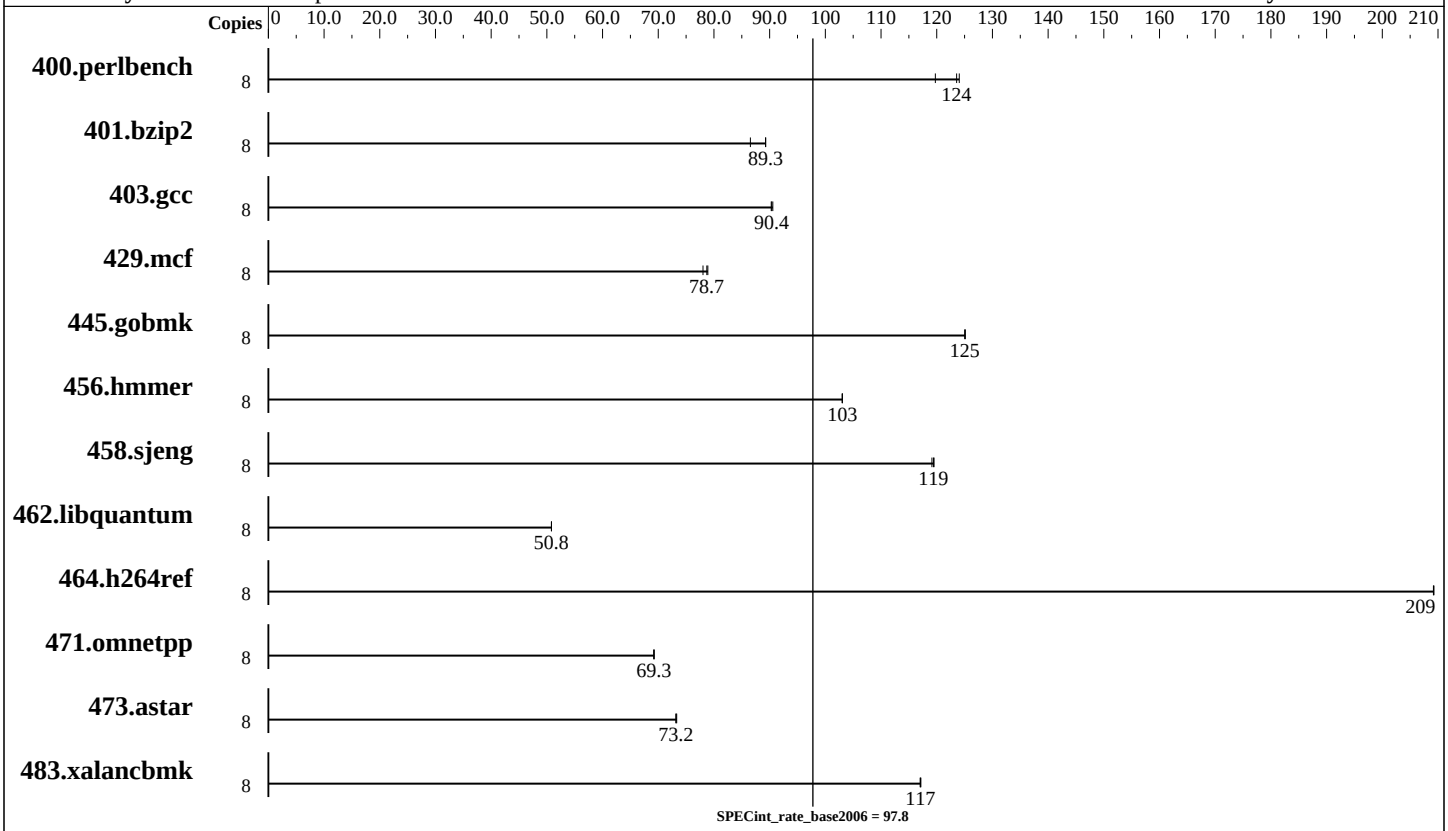
IBM System x3400 (Intel Xeon E5420)

SPECint®_rate2006 = Not Run

SPECint_rate_base2006 = 97.8

CPU2006 license: 11
Test sponsor: IBM Corporation
Tested by: IBM Corporation

Test date: Mar-2008
Hardware Availability: Jan-2008
Software Availability: Nov-2007



Hardware

CPU Name:	Intel Xeon E5420
CPU Characteristics:	1333MHz system bus
CPU MHz:	2500
FPU:	Integrated
CPU(s) enabled:	8 cores, 2 chips, 4 cores/chip
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	12 MB I+D on chip per chip, 6 MB shared / 2 cores
L3 Cache:	None
Other Cache:	None
Memory:	16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem:	1 x 80 GB SATA, 7200 RPM
Other Hardware:	None

Software

Operating System:	SuSE Linux Enterprise Server 10 (x86_64), Kernel 2.6.16.21-0.8-smp
Compiler:	Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel:	No
File System:	ReiserFS
System State:	Multi-user, run level 3
Base Pointers:	32-bit
Peak Pointers:	Not Applicable
Other Software:	MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	653	120	630	124	**633**	**124**							
401.bzip2	8	892	86.5	865	89.3	**865**	**89.3**							
403.gcc	8	711	90.6	**713**	**90.4**	713	90.3							
429.mcf	8	925	78.9	**927**	**78.7**	935	78.0							
445.gobmk	8	**671**	**125**	671	125	671	125							
456.hmmer	8	725	103	724	103	**724**	**103**							
458.sjeng	8	813	119	**811**	**119**	810	120							
462.libquantum	8	3262	50.8	3261	50.8	**3261**	**50.8**							
464.h264ref	8	846	209	**846**	**209**	846	209							
471.omnetpp	8	722	69.3	**722**	**69.3**	723	69.2							
473.astar	8	767	73.2	766	73.3	**767**	**73.2**							
483.xalancbmk	8	**471**	**117**	471	117	472	117							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
All benchmarks compiled in 32-bit mode
Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
taskset utility used to bind CPU(s) to processes
This result is measured on an IBM System x3500 Server. Note
that the IBM System x3500 and IBM System x3400 are electrically
equivalent.
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:
```
-fast -inline-calloc -opt-malloc-options=3
```

C++ benchmarks:
```
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
-L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap
```

Base Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags file that was used to format this result can be browsed at
`http://www.spec.org/cpu2006/flags/Intel-ic10.1-INT-ia32-linux-flags.html`

You can also download the XML flags source by saving the following link:
`http://www.spec.org/cpu2006/flags/Intel-ic10.1-INT-ia32-linux-flags.xml`

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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