**Fujitsu Siemens Computers**

**PRIMERGY TX300 S4, Intel Xeon X5260, 3.33 GHz**

**CPU2006 license: 22**
**Test sponsor: Fujitsu Siemens Computers**
**Tested by: Fujitsu Siemens Computers**

**Test date:** Jan-2008
**Hardware Availability:** Dec-2007
**Software Availability:** Nov-2007

### SPECint®_rate2006 = 81.0

<table>
<thead>
<tr>
<th>Test</th>
<th>SPECint_rate_base2006 = 68.8</th>
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</thead>
<tbody>
<tr>
<td>400.perlbench</td>
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<tr>
<td>401.bzip2</td>
<td></td>
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<tr>
<td>403.gcc</td>
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<td>429.mcf</td>
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<td>445.gobmk</td>
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<td>458.sjeng</td>
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<td>462.libquantum</td>
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<td>473.astar</td>
<td></td>
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<tr>
<td>483.xalancbmk</td>
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</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon X5260
- **CPU Characteristics:** 1333 MHz system bus
- **CPU MHz:** 3333
- **FPU:** Integrated
- **CPU(s) enabled:** 4 cores, 2 chips, 2 cores/chip
- **CPU(s) orderable:** 1.2 chips
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 6 MB I+D on chip per chip
- **L3 Cache:** None
- **Other Cache:** None
- **Memory:** 16 GB (8x2 GB PC2-5300F, 2 rank, CAS 5-5-5, with ECC)
- **Disk Subsystem:** Seagate ST973451SS (SAS, 73GB, 15000rpm)
- **Other Hardware:** None

**Software**

- **Operating System:** SUSE Linux Enterprise Server 10 (x86_64) SP1, Kernel 2.6.16.46-0.12-smp
- **Compiler:** Intel C++ Compiler for Linux32 and Linux64 Version 10.1 - Build 20070725
- **Auto Parallel:** Yes
- **File System:** ext2
- **System State:** Multiuser, Runlevel 3
- **Base Pointers:** 32-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** MicroQuill SmartHeap Library, Version 8.1 binutils-2.17.tar.gz, Version 2.17
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**SPEC CINT2006 Result**

**SPECint_rate2006 =** 81.0  
**SPECint_rate_base2006 =** 68.8

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**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Base Seconds</th>
<th>Ratio</th>
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<td>325</td>
<td>84.9</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

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### Operating System Notes

'OMP_NUM_THREADS' set to number of cores (default)

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### General Notes

This result has been produced with binaries provided and compiled by Intel.

All binaries were built with 32-bit Intel compiler except: 401.bzip2 and 456.hmmer in peak were built with 64-bit Intel compiler by changing the path for include and library files.

**BIOS configuration:**  
Adjacent Sector Prefetch = Disable

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http://www.fujitsu-siemens.com

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### Base Compiler Invocation

**C benchmarks:**  
icc

**C++ benchmarks:**  
icpc
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Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
- fast -inline-calloc -opt-malloc-options=3
C++ benchmarks:
- -xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
- -L/home/cmplr/usr3/alrahate/cpu2006.1.0/lib -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
ncc
401.bzip2: /home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/bin/ncc
- -L/home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/lib
- -I/home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/include
456.hmmer: /home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/bin/ncc
- -L/home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/lib
- -I/home/cmplr/usr3/alrahate/compilers/ic10.1mainline/20070725/Linux64/include

C++ benchmarks:
nicpc

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX

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Peak Portability Flags (Continued)

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -fast -ansi-alias
-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -fast -prefetch

403.gcc: -fast -inline-cALLOC -opt-mALLOC-options=3

429.mcf: -fast -prefetch

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xT -O2 -ipo
-no-preC-div -ansi-alias

456.hmmer: -fast -unroll2 -ansi-alias -opt-multi-version-aggressive

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -fast -unroll4

462.libquantum: -fast -unroll4 -Ob0 -prefetch
-opt-streaming-stores always -vec-guard-write
-opt-malloc-options=3 -parallel -par-runtime-control

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -fast -unroll2
-ansi-alias

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xT -O3 -ipo
-no-preC-div -ansi-alias -opt-ra-region-strategy=block
-Wl,-z,muldefs
-L/home/cmplr/usr3/alrahate/cpu2006.1.0/lib -lsmartheap

473.astar: -prof-gen(pass 1) -prof-use(pass 2) -xT -O3 -ipo
-no-preC-div -ansi-alias -opt-ra-region-strategy=routine
-Wl,-z,muldefs
-L/home/cmplr/usr3/alrahate/cpu2006.1.0/lib -lsmartheap

483.xalancbmk: basepeak = yes
SPEC CINT2006 Result

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Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.01.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.01.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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