



SPEC® CINT2006 Result

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IBM Corporation

SPECint®_rate2006 = Not Run

IBM BladeCenter HS21 (Intel Xeon E5430)

SPECint_rate_base2006 = 101

CPU2006 license: 11

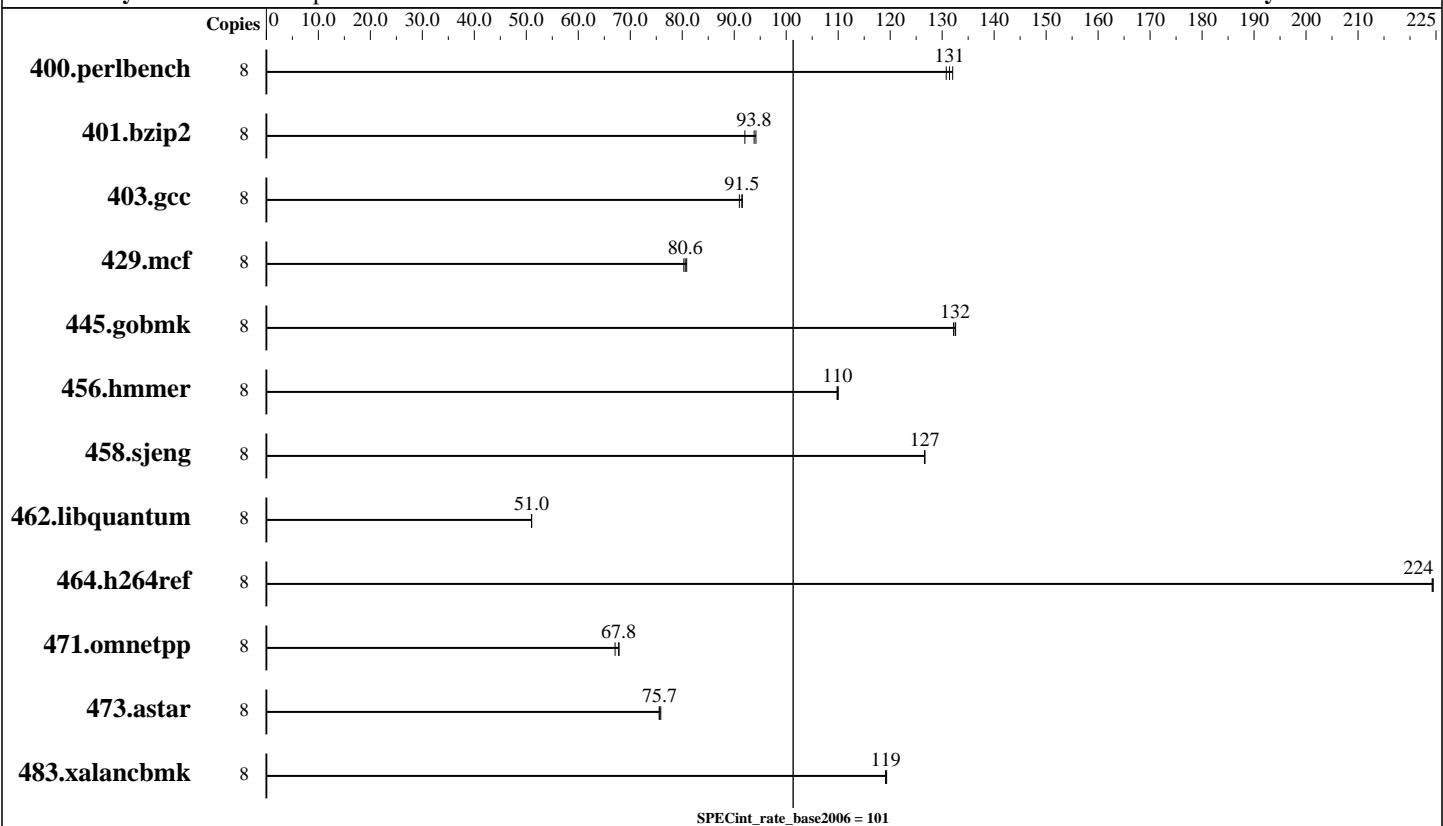
Test sponsor: IBM Corporation

Tested by: IBM Corporation

Test date: Dec-2007

Hardware Availability: Jan-2008

Software Availability: Nov-2007



Hardware

CPU Name: Intel Xeon E5430
CPU Characteristics: 1333MHz system bus
CPU MHz: 2666
FPU: Integrated
CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 12 MB I+D on chip per chip, 6 MB shared / 2 cores
L3 Cache: None
Other Cache: None
Memory: 16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem: 1 x 36 GB SAS, 10000 RPM
Other Hardware: None

Software

Operating System: SuSE Linux Enterprise Server 10 (x86_64), Kernel 2.6.16.21-0.8-smp
Compiler: Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel: No
File System: ReiserFS
System State: Multi-user, run level 3
Base Pointers: 32-bit
Peak Pointers: Not Applicable
Other Software: MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	598	131	592	132	<u>595</u>	<u>131</u>							
401.bzip2	8	820	94.2	839	92.0	<u>823</u>	<u>93.8</u>							
403.gcc	8	703	91.5	708	91.0	<u>704</u>	<u>91.5</u>							
429.mcf	8	909	80.3	902	80.9	<u>905</u>	<u>80.6</u>							
445.gobmk	8	633	133	635	132	<u>633</u>	<u>132</u>							
456.hammer	8	679	110	680	110	678	110							
458.sjeng	8	764	127	765	127	764	127							
462.libquantum	8	3249	51.0	3249	51.0	3250	51.0							
464.h264ref	8	789	224	789	224	789	224							
471.omnetpp	8	737	67.8	745	67.1	<u>738</u>	<u>67.8</u>							
473.astar	8	743	75.6	740	75.9	<u>742</u>	<u>75.7</u>							
483.xalancbmk	8	463	119	463	119	463	119							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

All benchmarks compiled in 32-bit mode

Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
taskset utility used to bind CPU(s) to processes

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-fast -inline-calloc -opt-malloc-options=3

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Base Optimization Flags (Continued)

C++ benchmarks:

```
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs  
-L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap
```

Base Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

The flags file that was used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.html>

You can also download the XML flags source by saving the following link:

<http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.xml>

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.0.

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