SPEC® CINT2006 Result

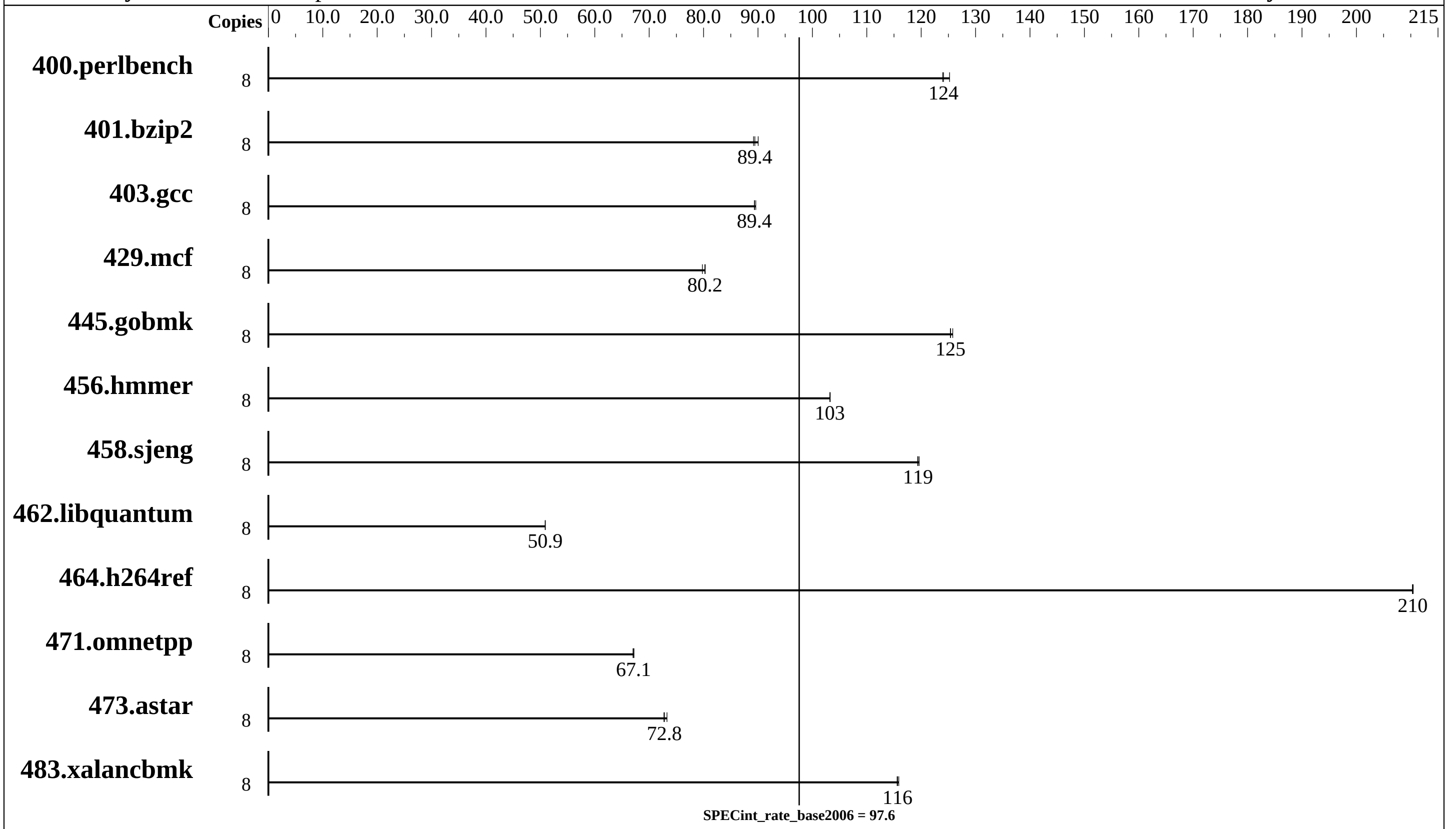
IBM Corporation

SPECint®_rate2006 = Not Run

IBM BladeCenter HS21 (Intel Xeon E5420)

SPECint_rate_base2006 = 97.6

CPU2006 license:	11	**Test date:**	Dec-2007
Test sponsor:	IBM Corporation	**Hardware Availability:**	Jan-2008
Tested by:	IBM Corporation	**Software Availability:**	Nov-2007



Hardware

CPU Name:	Intel Xeon E5420
CPU Characteristics:	1333MHz system bus
CPU MHz:	2493
FPU:	Integrated
CPU(s) enabled:	8 cores, 2 chips, 4 cores/chip
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	12 MB I+D on chip per chip, 6 MB shared / 2 cores
L3 Cache:	None
Other Cache:	None
Memory:	16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem:	1 x 36 GB SAS, 10000 RPM
Other Hardware:	None

Software

Operating System:	SuSE Linux Enterprise Server 10 (x86_64), Kernel 2.6.16.21-0.8-smp
Compiler:	Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel:	No
File System:	ReiserFS
System State:	Multi-user, run level 3
Base Pointers:	32-bit
Peak Pointers:	Not Applicable
Other Software:	MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	630	124	624	125	**630**	**124**							
401.bzip2	8	857	90.0	866	89.2	**863**	**89.4**							
403.gcc	8	**721**	**89.4**	721	89.3	719	89.6							
429.mcf	8	**909**	**80.2**	915	79.8	909	80.3							
445.gobmk	8	667	126	**669**	**125**	669	125							
456.hmmer	8	**723**	**103**	723	103	723	103							
458.sjeng	8	811	119	**811**	**119**	809	120							
462.libquantum	8	**3256**	**50.9**	3258	50.9	3256	50.9							
464.h264ref	8	841	210	842	210	**842**	**210**							
471.omnetpp	8	**745**	**67.1**	746	67.0	744	67.2							
473.astar	8	766	73.3	772	72.7	**771**	**72.8**							
483.xalancbmk	8	476	116	478	116	**477**	**116**							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
All benchmarks compiled in 32-bit mode
Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
taskset utility used to bind CPU(s) to processes
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:
`-fast -inline-calloc -opt-malloc-options=3`

Continued on next page

Base Optimization Flags (Continued)

C++ benchmarks:

```
-xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
-L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap
```

Base Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.13.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.0.
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