SPEC® CINT2006 Result

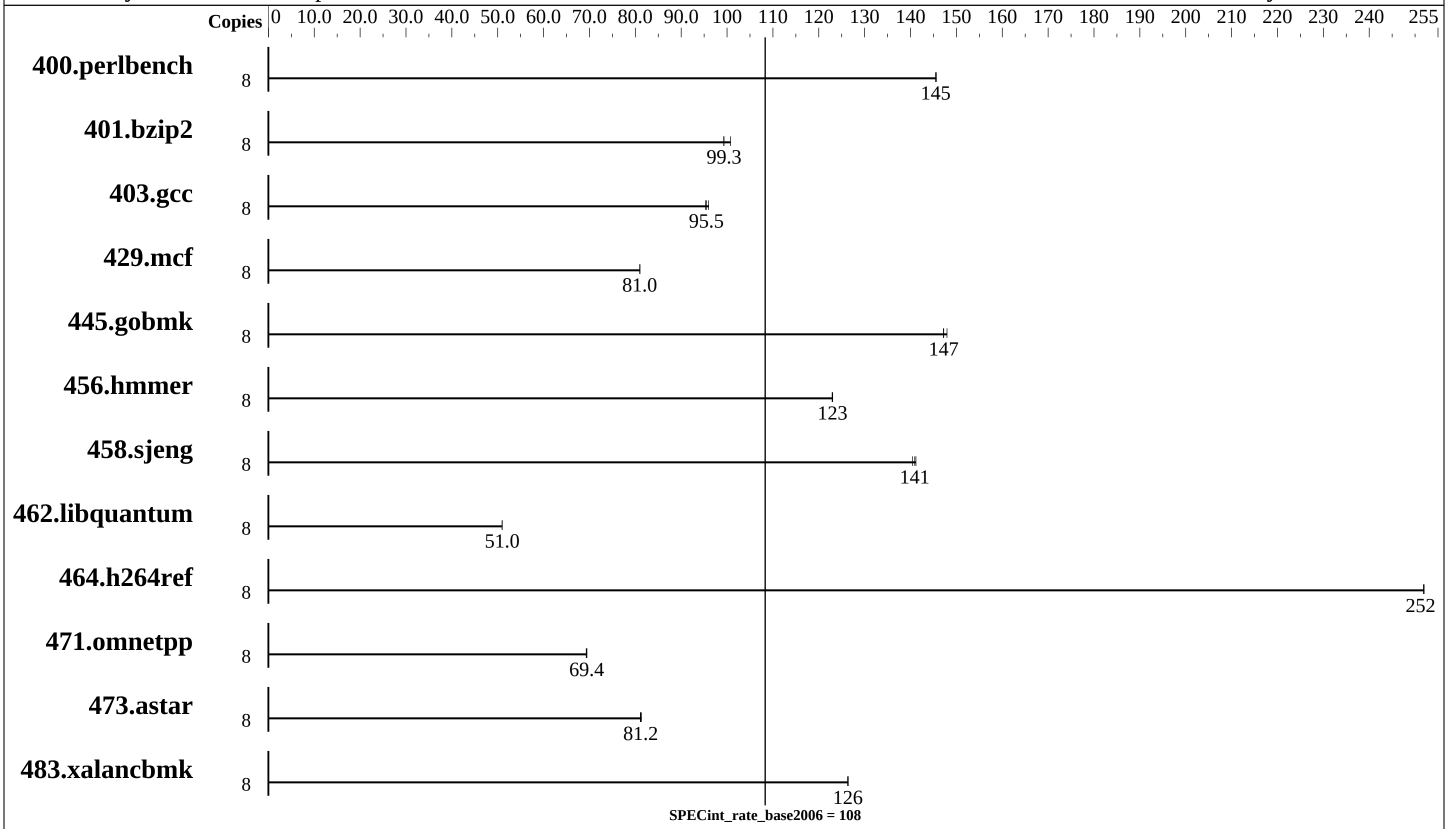
IBM Corporation

SPECint®_rate2006 = Not Run

IBM BladeCenter HS21 XM (Intel Xeon E5450)

SPECint_rate_base2006 = 108

CPU2006 license:	11	**Test date:**	Nov-2007
Test sponsor:	IBM Corporation	**Hardware Availability:**	Jan-2008
Tested by:	IBM Corporation	**Software Availability:**	Nov-2007



Hardware

CPU Name:	Intel Xeon E5450
CPU Characteristics:	1333MHz system bus
CPU MHz:	3000
FPU:	Integrated
CPU(s) enabled:	8 cores, 2 chips, 4 cores/chip
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	12 MB I+D on chip per chip, 6 MB shared / 2 cores
L3 Cache:	None
Other Cache:	None
Memory:	16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem:	1 x 36 GB SAS, 10000 RPM
Other Hardware:	None

Software

Operating System:	SLES10 (x86_64), 2.6.16.21-0.8-smp
Compiler:	Intel C++ Compiler 10.1 for Linux Build 20070913 Package ID: l_cc_p_10.1.008
Auto Parallel:	No
File System:	ReiserFS
System State:	Multi-user, run level 3
Base Pointers:	32-bit
Peak Pointers:	Not Applicable
Other Software:	MicroQuill SmartHeap 8.1 Binutils 2.17.50.0.15

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	537	146	537	145	**537**	**145**							
401.bzip2	8	**777**	**99.3**	778	99.3	766	101							
403.gcc	8	676	95.3	**674**	**95.5**	671	96.0							
429.mcf	8	901	81.0	**901**	**81.0**	901	81.0							
445.gobmk	8	570	147	**570**	**147**	567	148							
456.hmmer	8	**607**	**123**	607	123	607	123							
458.sjeng	8	689	140	686	141	**687**	**141**							
462.libquantum	8	3251	51.0	**3252**	**51.0**	3252	51.0							
464.h264ref	8	703	252	**703**	**252**	703	252							
471.omnetpp	8	**720**	**69.4**	722	69.3	720	69.4							
473.astar	8	**692**	**81.2**	690	81.3	693	81.1							
483.xalancbmk	8	**437**	**126**	437	126	437	126							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
All benchmarks compiled in 32-bit mode except 401.bzip2 and 456.hmmer,
for peak, are compiled in 64-bit mode
Hardware Sector Prefetch Disabled and Adjacent Sector Prefetch Disabled
OMP_NUM_THREADS set to number of cores
KMP_AFFINITY set to physical,0
KMP_STACKSIZE set to 64M
taskset utility used to bind CPU(s) to processes
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

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Base Optimization Flags

C benchmarks:
    -fast -inline-calloc -opt-malloc-options=3

C++ benchmarks:
    -xT -ipo -O3 -no-prec-div -Wl,-z,muldefs
    -L/spec/users/rahul/cpu2006.1.0/lib -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.31.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.31.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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