Supermicro
Motherboard PDSMA+

SPECint_rate2006 = 39.9
SPECint_rate_base2006 = 33.1

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CPU2006 license: 001176
Test date: Jun-2007
Test sponsor: Supermicro
Hardware Availability: May-2007
Software Availability: May-2007

Hardware

CPU Name: Intel Core 2 Extreme QX6700
CPU Characteristics: 2.66GHz 1066 MHz System Bus
CPU MHz: 2660
FPU: Integrated
CPU(s) enabled: 4 cores, 1 chip, 4 cores/chip
CPU(s) orderable: 1 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 8 MB I+D on chip per chip, 4 MB shared / 2 cores
L3 Cache: None
Other Cache: None
Memory: 8 GB (4 X 2GB ECC PC2-5300, CL5, DDR2)
Disk Subsystem: 250GB SATA, 7200RPM
Other Hardware: None

Software

Compiler: Intel C++ Compiler for IA32 version 10.0
Build 20070426 Package ID: W_CC_P_10.0.025
Microsoft Visual Studio .Net 2003 (for libraries)
Auto Parallel: No
File System: NTFS
System State: Default
Base Pointers: 32-bit
Peak Pointers: 32-bit
Other Software: SmartHeap Library Version 8.0 from http://www.microquill.com/
Supermicro Motherboard PDSMA+

SPECint_rate2006 = 39.9
SPECint_rate_base2006 = 33.1

RESULTS TABLE

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

GENERAL NOTES

Tested systems can be used with CSE-733T-450 case, Product description located as of http://www.supermicro.com/products/motherboard/Xeon3000/3000/PDSMA+.cfm
The system bus runs at 1066 MHz
"start /b /wait /affinity" used to bind processes to CPUs.

BASE COMPILER INVOCATION

C benchmarks:
  icl -Qvc7.1 -Qc99

C++ benchmarks:
  icl -Qvc7.1

BASE PORTABILITY FLAGS

403.gcc: -DSPEC_CPU_WIN32
464.h264ref: -DSPEC_CPU_NO_INNTYPES -DWIN32

BASE OPTIMIZATION FLAGS

C benchmarks:
- fast /F512000000 shlw32m.lib -link /FORCE:MULTIPLE

Continued on next page
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Test date: Jun-2007
Hardware Availability: May-2007
Software Availability: May-2007

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**Base Optimization Flags (Continued)**

C++ benchmarks:
-\texttt{-fast -Qcxx\_features /F512000000 shlw32m.lib}
-\texttt{-link /FORCE\_MULTIPLE}

---

**Base Other Flags**

C benchmarks:
-403.gcc: \texttt{-Dalloca=_alloca}

---

**Peak Compiler Invocation**

C benchmarks:
-\texttt{icl -Qvc7.1 -Qc99}

C++ benchmarks:
-\texttt{icl -Qvc7.1}

---

**Peak Portability Flags**

-403.gcc: \texttt{-DSPEC\_CPU\_WIN32}
-464.h264ref: \texttt{-DSPEC\_CPU\_NO\_INTTYPES -DWIN32}

---

**Peak Optimization Flags**

C benchmarks:
-400.perlbench: \texttt{-Qprof\_gen(pass 1) -Qprof\_use(pass 2) -fast -Qansi\_alias}
-\texttt{-Qprefetch /F512000000 shlw32m.lib}
-\texttt{-link /FORCE\_MULTIPLE}

-401.bzip2: \texttt{-Qprof\_gen(pass 1) -Qprof\_use(pass 2) -fast /F512000000}
-\texttt{shlw32m.lib -link /FORCE\_MULTIPLE}

-403.gcc: \texttt{-Qprof\_gen(pass 1) -Qprof\_use(pass 2) -fast /F512000000}
-\texttt{-link /FORCE\_MULTIPLE}

-429.mcf: \texttt{basepeak = yes}

-445.gobmk: \texttt{-Qprof\_gen(pass 1) -Qprof\_use(pass 2) -QxT -O2 -Qipo -Qprec\_div- -Qansi\_alias /F512000000}
-\texttt{-link /FORCE\_MULTIPLE}

Continued on next page
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Software Availability: May-2007

Peak Optimization Flags (Continued)

456.hmmer: 
-fflag_gen(pass 1) 
-fflag_use(pass 2) 
-round 128
-Qansi-alias /F512000000 shlw32m.lib 
-fflag_link /FORCE:MULTIPLE

458.sjeng: 
-fflag_gen(pass 1) 
-fflag_use(pass 2) 
-round 128
-Qansi-alias /F512000000 shlw32m.lib 
-fflag_link /FORCE:MULTIPLE

462.libquantum: 
-fflag_gen(pass 1) 
-fflag_use(pass 2) 
-round 128
-Qansi-alias /F512000000 shlw32m.lib 
-fflag_link /FORCE:MULTIPLE

464.h264ref: Same as 456.hmmer

C++ benchmarks:
-fflag_gen(pass 1) 
-fflag_use(pass 2) 
-round 128
-Qansi-alias /F512000000 shlw32m.lib 
-fflag_link /FORCE:MULTIPLE

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.18.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/Intel-ic10-ia32-intel64-linux-flags.20090714.18.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.0.