## Hewlett-Packard Company
### AlphaServer ES80 7/1000

**SPECfp2000** = 1288  
**SPECfp_base2000** = 975

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Reference Time</th>
<th>Base Runtime</th>
<th>Base Ratio</th>
<th>Runtime</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>168.wupwise</td>
<td>1600</td>
<td>210</td>
<td>760</td>
<td>86.7</td>
<td>1846</td>
</tr>
<tr>
<td>171.swim</td>
<td>3100</td>
<td>99.1</td>
<td>3130</td>
<td>99.1</td>
<td>3130</td>
</tr>
<tr>
<td>172.mgrid</td>
<td>1800</td>
<td>293</td>
<td>614</td>
<td>192</td>
<td>938</td>
</tr>
<tr>
<td>173.aplul</td>
<td>2100</td>
<td>159</td>
<td>1318</td>
<td>156</td>
<td>1345</td>
</tr>
<tr>
<td>177.mesa</td>
<td>1400</td>
<td>173</td>
<td>808</td>
<td>145</td>
<td>965</td>
</tr>
<tr>
<td>178.galgel</td>
<td>2900</td>
<td>158</td>
<td>1830</td>
<td>157</td>
<td>1851</td>
</tr>
<tr>
<td>179.art</td>
<td>2600</td>
<td>149</td>
<td>1741</td>
<td>92.4</td>
<td>2814</td>
</tr>
<tr>
<td>183.equake</td>
<td>1300</td>
<td>290</td>
<td>449</td>
<td>94.2</td>
<td>1381</td>
</tr>
<tr>
<td>187.facerec</td>
<td>1900</td>
<td>198</td>
<td>961</td>
<td>178</td>
<td>1069</td>
</tr>
<tr>
<td>188.ammp</td>
<td>2200</td>
<td>345</td>
<td>638</td>
<td>299</td>
<td>735</td>
</tr>
<tr>
<td>189.lucas</td>
<td>2000</td>
<td>150</td>
<td>1331</td>
<td>138</td>
<td>1453</td>
</tr>
<tr>
<td>191.fma3d</td>
<td>2100</td>
<td>238</td>
<td>883</td>
<td>177</td>
<td>1186</td>
</tr>
<tr>
<td>200.sixtrack</td>
<td>1100</td>
<td>272</td>
<td>404</td>
<td>252</td>
<td>437</td>
</tr>
<tr>
<td>301.apsi</td>
<td>2600</td>
<td>241</td>
<td>1078</td>
<td>225</td>
<td>1158</td>
</tr>
</tbody>
</table>

### Hardware
- **CPU**: Alpha 21364
- **CPU MHz**: 1000
- **FPU**: Integrated
- **CPU(s) enabled**: 1 core, 1 chip, 1 core/chip
- **CPU(s) orderable**: 2 to 8
- **Parallel**: No
- **Primary Cache**: 64KB(I)+64KB(D) on chip
- **Secondary Cache**: 1.75MB on chip per CPU
- **L3 Cache**: None
- **Other Cache**: None
- **Memory**: 4GB
- **Disk Subsystem**: 36GB SCSI
- **Other Hardware**: None

### Software
- **Operating System**: Tru64 UNIX V5.1B (Rev. 2650) +IPK
- **Compiler**: Compaq C V6.5-011-48C5K  
  Spike V5.2 (506A)  
  Compaq Fortran V5.5-2602-48C8L  
  Compaq Fortran 77 V5.5-2602-48C8L  
  KAP Fortran V4.3 k3105171 000607  
  KAP Fortran 77 V4.1 k310440 980926  
  KAP C V4.1 k010726 000607
- **File System**: ufs
- **System State**: Multi-user

### Notes/Tuning Information

**Baseline**
- C: cc -arch ev7 -fast -O4 ONESTEP
- Fortran: f90 -arch ev7 -fast -O5 ONESTEP

**Peak**
- All use -arch ev7 -non_shared ONESTEP
- except these (which use only the tunings shown below):
  - 173.applu 188.ammp 191.fma3d

**Individual benchmark tuning**:
- 168.wupwise: kf77 -call_shared -inline all -tune ev67
  - unroll 12 -automatic -align commons -arch ev67
  - -fkapargs=' -aggressive=c -fuse
  - -fusesecondary=1 -so=2 -r=1 -o=1 -interleave
  - -ur=6 -ur2=060 ' +PFB
- 171.swim: same as base
- 172.mgrid: kf90 -call_shared -arch generic -O5 -inline
Hewlett-Packard Company
AlphaServer ES80 7/1000

SPECfp2000 = 1288
SPECfp_base2000 = 975

Notes/Tuning Information (Continued)

manual -nopipeline -transform_loops -unroll 9 -automatic
-fkapargs='-aggressive=a -fuse -interleave
-ur=2 -ur3=5 -cachesize=128,16000 ' +PFB

173.applu: kf90 -05 -transform_loops
-fkapargs=' -o=0 -notransform_loops -ur=14
-ur2=260 -ur3=18' +PPB

177.mesa: kcc -fast -04 +CFB +IFB

178.galgel: f90 -05 -fast -unroll 5 -automatic

179.art: kcc -assume whole_program -ldensemalloc
-call_shared -assume restricted_pointers
-unroll 16 -inline none -ckapargs=' -f -fuselevel=1 -ur=3' +PPB

183.equake: cc -call_shared -arch generic -fast -04
-ldensemalloc -assume restricted_pointers
-inline speed -unroll 13 -xtaso_short +PFB

187.facevec: f90 -04 -nopipeline -inline all
-non_shared -speculate all -unroll 7
-automatic -assume accuracy_sensitive
-math_library fast +IFB

188.ammp: cc -arch host -04 -ifo -assume nomath_errno
-assume trusted_short_alignment -fp reorder
-readonly_strings -ldensemalloc -xtaso_short
-assume restricted_pointers -unroll 9
-inline speed +CFB +IFB +PFB

189.lucas: kf90 -05 -fkapargs=' -ur=1' +PFB

191.fma3d: kf90 -arch ev6 -non_shared -04 -transform_loops
-fkapargs=' -cachesize=128,16000 ' +PFB

200.sixtrack: f90 -fast -05 -assume accuracy_sensitive
-notransform_loops +PFB

301.apsi: kf90 -05 -inline none -call_shared -speculate all
-align commons -fkapargs=' -aggressive=ab
-tune=ev5 -f -fuse -ur=1 -ur2=60 -ur3=20
-cachesize=128,16000'

Most benchmarks are built using one or more types of
profile-driven feedback. The types used are designated
by abbreviations in the notes:

+CFB: Code generation is optimized by the compiler, using
feedback from a training run. These commands are
done before the first compile (in phase "fdo_pre0"):

```bash
mkdir /tmp/pp
rm -f /tmp/pp/$(baseexe)*

and these flags are added to the first and second compiles:

PASS1_CFLAGS = -prof_gen_noopt -prof_dir /tmp/pp
PASS2_CFLAGS = -prof_use -prof_dir /tmp/pp
```

(Peak builds use /tmp/pp above; base builds use /tmp/pb.)

+IFB: Icache usage is improved by the post-link-time optimizer
Spike, using feedback from a training run. These commands
are used (in phase "fdo_postN"):

```bash
mkdir /tmp/pp
rm -f /tmp/pp/$(baseexe)*
```

and these flags are added to the first and second compiles:

```bash
PASS1_CFLAGS = -prof_gen_noopt -prof_dir /tmp/pp
PASS2_CFLAGS = -prof_use -prof_dir /tmp/pp
```

(Peak builds use /tmp/pp above; base builds use /tmp/pb.)
Hewlett-Packard Company
AlphaServer ES80 7/1000

SPECfp2000 = 1288
SPECfp_base2000 = 975

Notes/Tuning Information (Continued)

mv ${baseexe} oldexe
spike oldexe -feedback oldexe -o ${baseexe}

+PFB: Prefetches are improved by the post-link-time optimizer
Spike, using feedback from a training run. These
commands are used (in phase "fdo_post_makeN"):

    rm -f *Counts*
    mv ${baseexe} oldexe
    pixie -stats dstride oldexe 1>pixie.out 2>pixie.err
    mv oldexe.pixie ${baseexe}

A training run is carried out (in phase "fdo_runN"), and
then this command (in phase "fdo_postN"):

    spike oldexe -fb oldexe -stride_prefetch -o ${baseexe}

When Spike is used for both Icache and Prefetch improvements,
only one spike command is actually issued, with the Icache
options followed by the Prefetch options.

vm:

    vm_bigpg_enabled = 1
    vm_bigpg_thresh=16
    vm_swap_eager = 0

proc:

    max_per_proc_address_space = 0x400000000000
    max_per_proc_data_size = 0x400000000000
    max_per_proc_stack_size = 0x400000000000
    max_proc_per_user = 2048
    max_threads_per_user = 0
    maxusers = 16384
    per_proc_address_space = 0x400000000000
    per_proc_data_size = 0x400000000000
    per_proc_stack_size = 0x400000000000

Portability: galgel: -fixed

Information on UNIX V5.1B Patches can be found at

In the ES80, there are two cpus per shelf. Each cpu has
its own 4GB of memory. Neither of the cpus can be
physically removed. For 1 cpu results measured on a 2 cpu
system, one cpu was turned off at boot time using the
/etc/sysconfigtab setting "cpu_enabled_mask=0". The cpu's
4GB of memory was also physically removed.